

Studies on Channel Coupling and Floating Body Effects and Their Impacts on
Device Performance and Reliability in SOI MOSFET

A thesis submitted in partial fulfillment of the requirements for the degree of Doctor of
Philosophy at George Mason University

By

Franklin L. Duan

B.S. Electrical Engineering, Tsinghua University, Beijing, China, 1985

M.S. Electrical Engineering, Tsinghua University, Beijing, China, 1987

Director: Dimitris E. Ioannou, Professor
Department of Electrical and Computer Engineering

Fall 1998
George Mason University
Fairfax, Virginia

**STUDIES ON CHANNEL COUPLING AND FLOATING BODY EFFECTS AND
THEIR IMPACTS ON DEVICE PERFORMANCE AND RELIABILITY
IN SOI MOSFET**

by

Franklin L. Duan
A Dissertation
Submitted to the
Graduate Faculty
of
George Mason University
in Partial Fulfillment of
the Requirements for the Degree
of
Doctor of Philosophy
Information Technology

Committee:

_____ Dimitris E. Ioannou, Dissertation Director

_____ Rao V. Mulpuri

_____ Andrzej Z. Manitius

_____ Ariela Sofer

_____ David A. Schum

_____ Carl M. Harris, Associate Dean for
Graduate Studies and Research

_____ Lloyd J. Griffith, Dean, School of
Information Technology and Engineering

Date: _____

Spring 1998
George Mason University
Fairfax, Virginia

ACKNOWLEDGEMENT

I would like to express my gratitude to my advisor Professor Dimitris Ioannou for his able guidance and help during the whole Ph.D. program. Also I would appreciate my colleagues Andrzej Zaleski, Shankar Sinha, and Xuejun Zhao for their useful suggestions as well as contributions, directly and indirectly, to this thesis. Finally special thanks for the financial and technical support from NSF, NRL, Honeywell and Texas Instruments.

ABSTRACT

Studies on Channel Coupling & Floating Body Effects and Their Impacts on Device Performance & Reliability in SOI MOSFET

Franklin L. Duan

George Mason University, 1998

Dissertation Director: Dr. Dimitris E. Ioannou

SOI MOSFET is one of the promising options for the future VLSI market due to its low power/high speed character and simplified technology with increased packing density. Yet some problems in device physics must be fully understood before SOI is implemented in industry. These problems are basically around the three features of SOI device: Two separate gates, channel coupling, and floating body effect. In this thesis, first an extensive study on the opposite-channel-based injection (OCBI) by manipulating these two gates is carried out by copious PISCES simulations. The results demonstrate that when stressing one channel, carriers can and are injected into the opposite gate. Under appropriate bias conditions pure hole/electron injection does take place, which can be used as a technique to characterize the electron/hole traps in SIMOX material. Secondly, the channel coupling effect was extensively carried out; both on electric field and impact ionization by numerical simulation, and on hot carrier degradation and single transistor latch-up from experiments. Results show that stronger coupling brings about a lower impact ionization, which lessens the substrate current and ameliorates the hot carrier degradation, but on the other hand modulates the electric field pattern in such a way to ease the activation of the parasitic bipolar transistor, which deteriorates the latch-up voltage. Thirdly the width effect of floating body effect was analyzed by a two-dimensional simulation which mimics its three dimensional features. Results reveal that there is considerably higher carrier generation

near the edges of the channel, and more so for wider devices. Those simulation results were verified by the latch-up voltage measurement and hot carrier degradation test. Fourthly, a new FD SOI MOSFET structure is proposed, which holds the drawbacks of low channel mobility in the inversion mode and poor latch-up voltage in the accumulation mode. Moreover, the new device is more resistant to hot carrier degradation. Finally, the compatibility of LDD bulk technology to SOI was studied. Results show that the optimized LDD technology for bulk is not optimized for SOI due to the tradeoff between device reliability and the latch-up voltage.