

Studies on Channel Coupling and Floating
Body Effects and Their Impacts on Device
Performance and Reliability in SOI MOSFET

Presenter: Franklin L. Duan

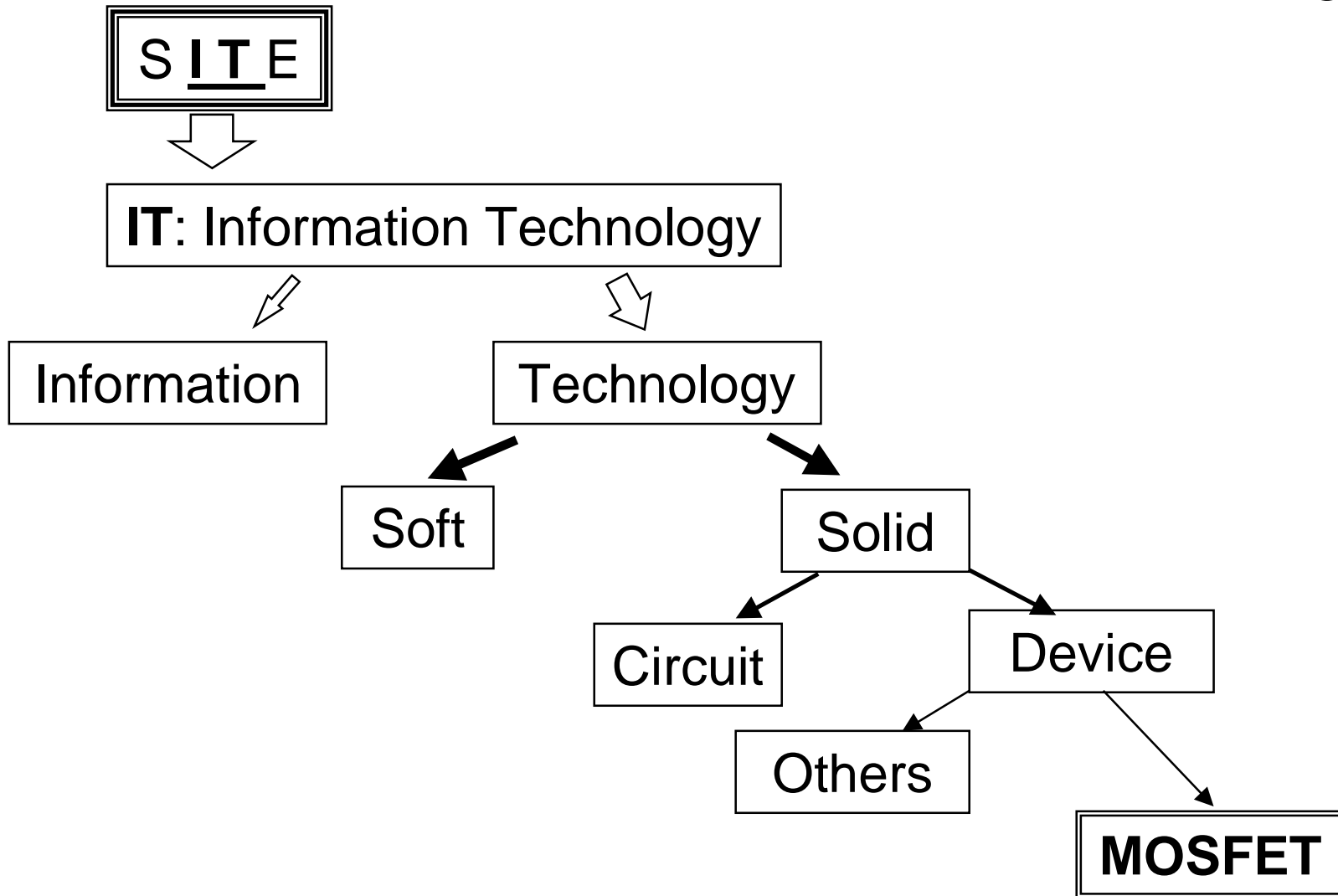
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Outline

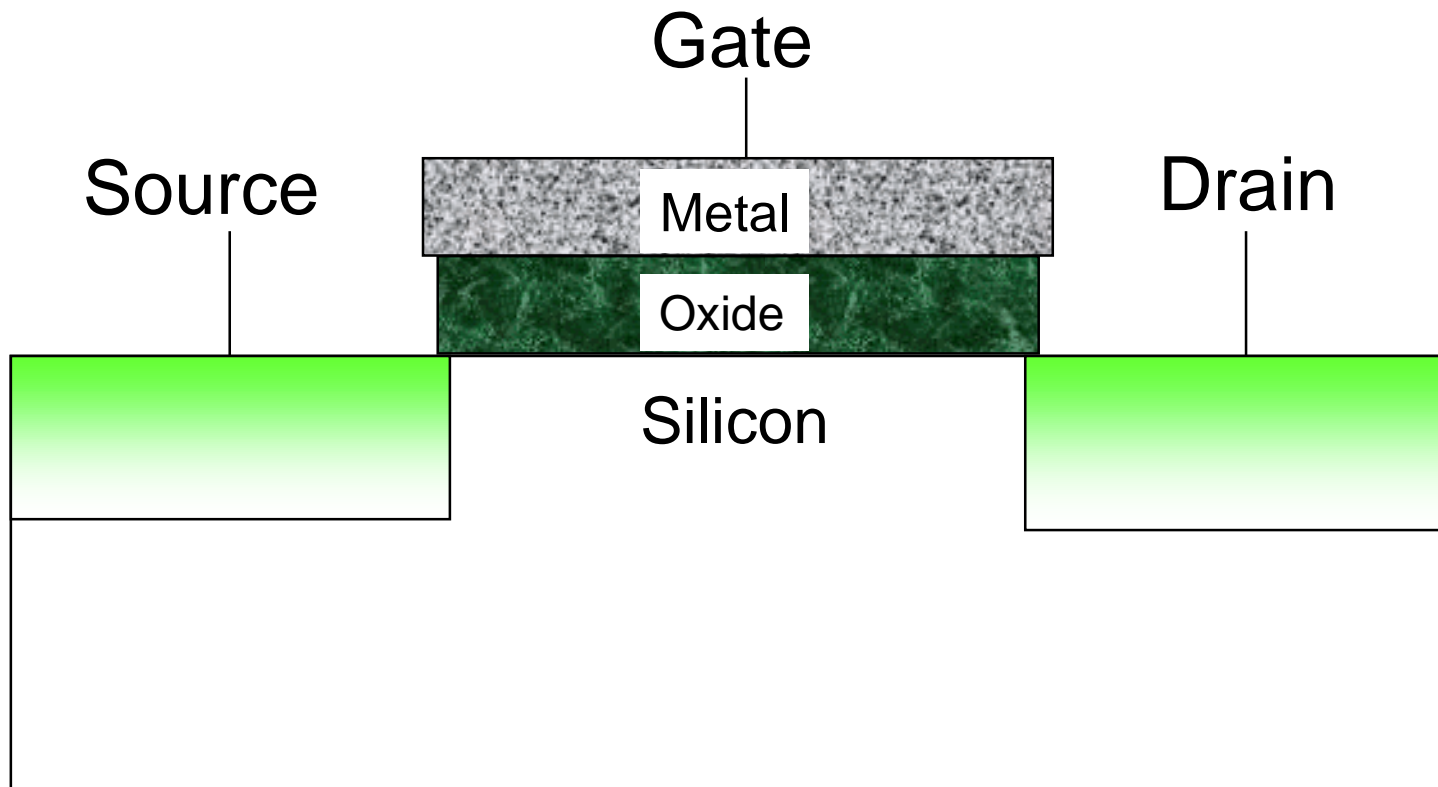
- MOSFET
- SOI MOSFET
- SOI Advantages
- SOI Basic Features/Problems
- Five Topics Studied
- Summary of the Results

Tree of Information Technology



MOSFET

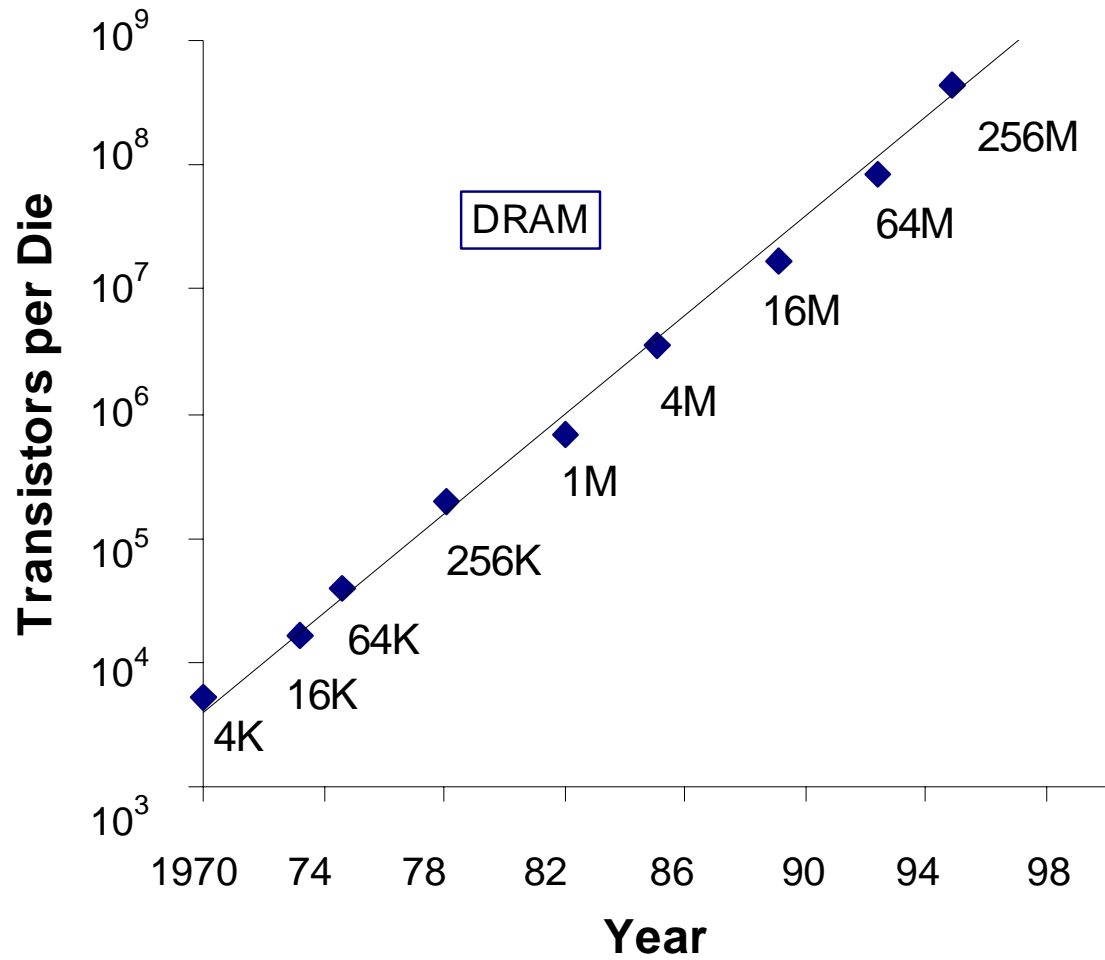
(Metal Oxide Silicon Field Effect Transistor)



Scaling-down Rule of MOSFET

		Scale factor ($K > 1$)
What to scale down	Surface dimension	$1/K$
	Vertical dimension	$1/K$
	Operating voltage	$1/K$
Results of the scaling down	Delay time	$1/K$
	Power dissipation	$1/K^2$
	Power-delay product	$1/K^3$

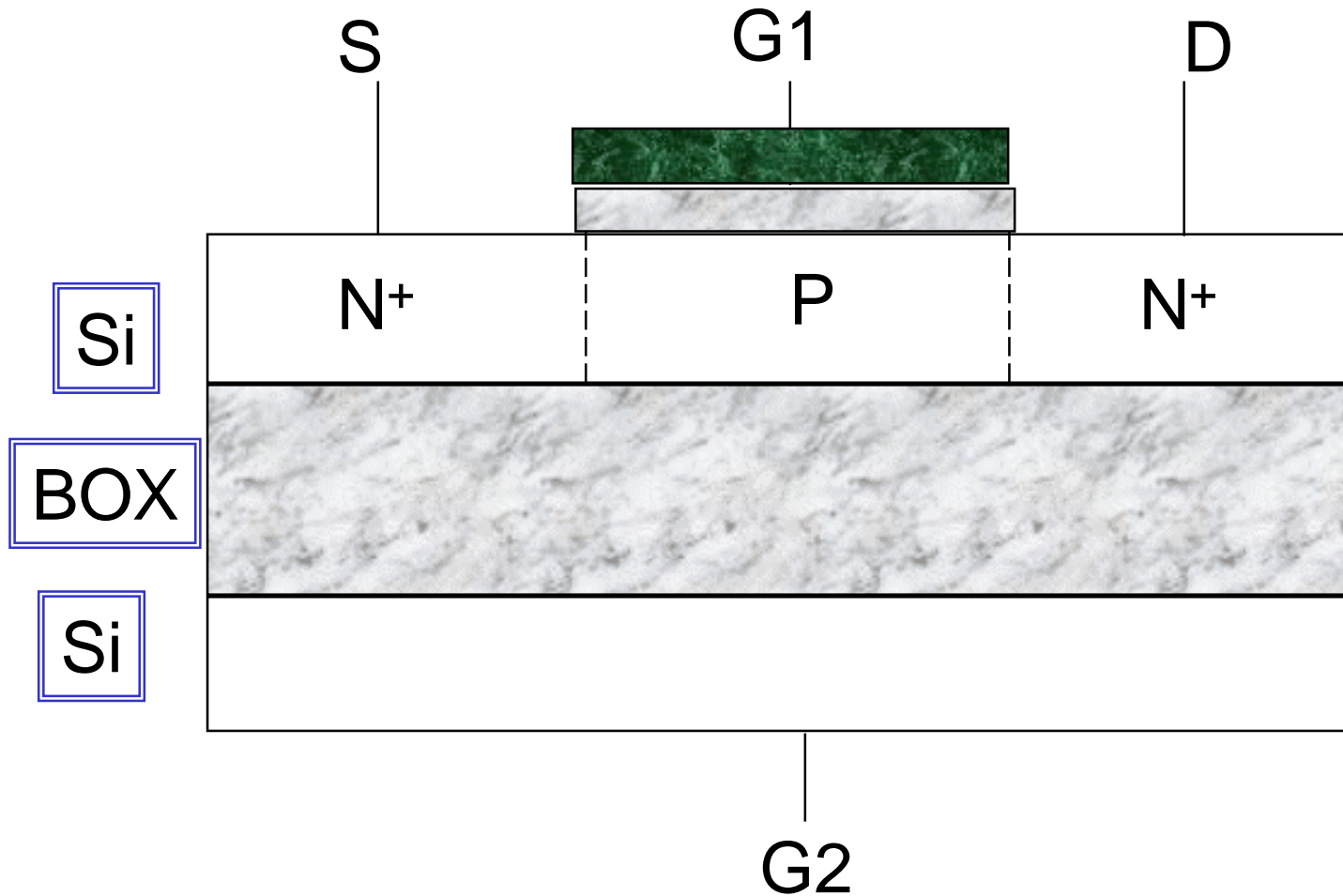
Moore's Law of VLSI



Side Effects of Scaling-down

- Hot carrier degradation due to the increased electric field and hot carrier injections
- Leakage current higher with increased driving current and higher capacitance

SOI (Silicon On Insulator) MOSFET



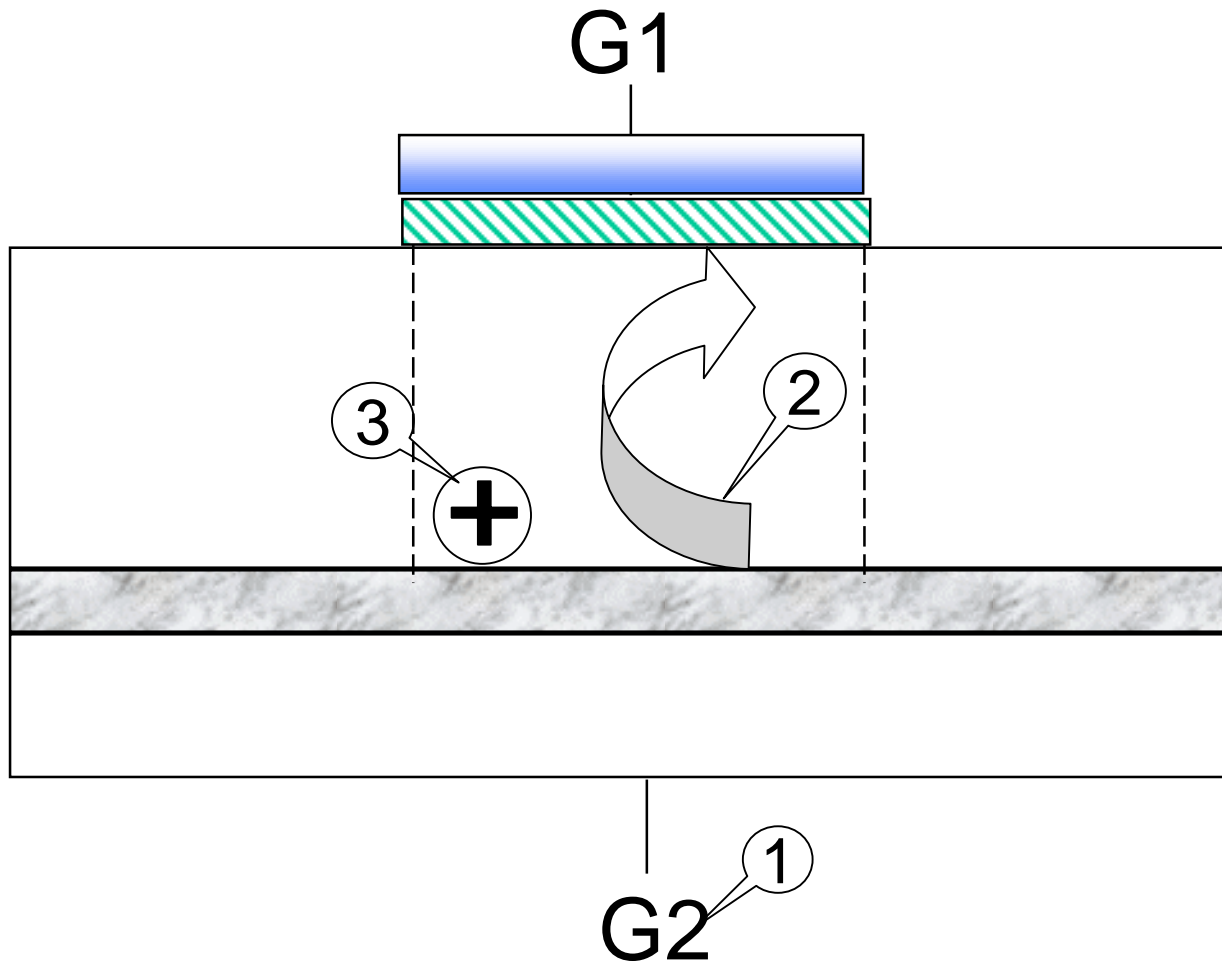
SOI Advantages

- Radiation hardness
- Low power/high speed
 - Reduction in parasitic capacitance
 - Improved subthreshold slope
- Improved short channel effect
- CMOS latch-up free
- Increased ULSI packing density
- Simplified fabrication

SOI Three Basic Features in Device Physics

- Dual Gate control
- Channel Coupling
- Floating Body Effect

Three Basic Features of SOI



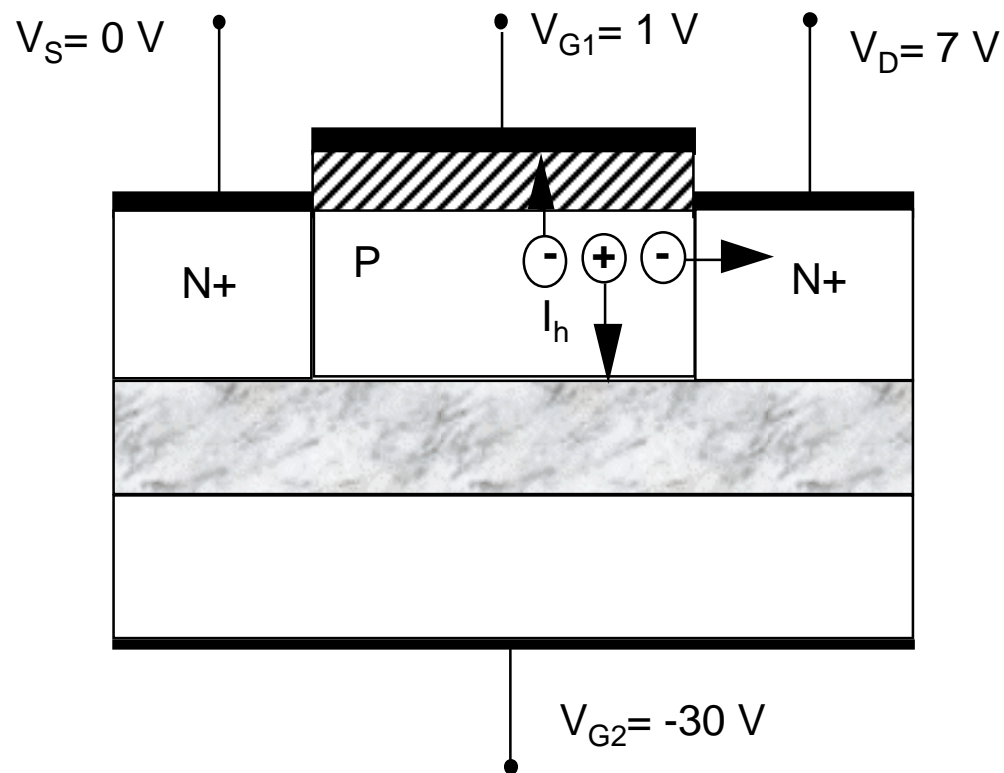
Five Topics Studied in the Thesis

- Dual gate control:
 - Opposite channel based-hot-carrier injection (OCBI) technique, unique tool for hot carrier study in SOI
- Channel coupling:
 - trade-off between hot carrier degradation and FBE
- Floating Body Effect (FBE):
 - abnormally higher impact ionization rate at the edges
- Two modes of operations in FD SOI:
 - a new mixed mode structure
- Bulk technology integration:
 - performance and reliability trade-off

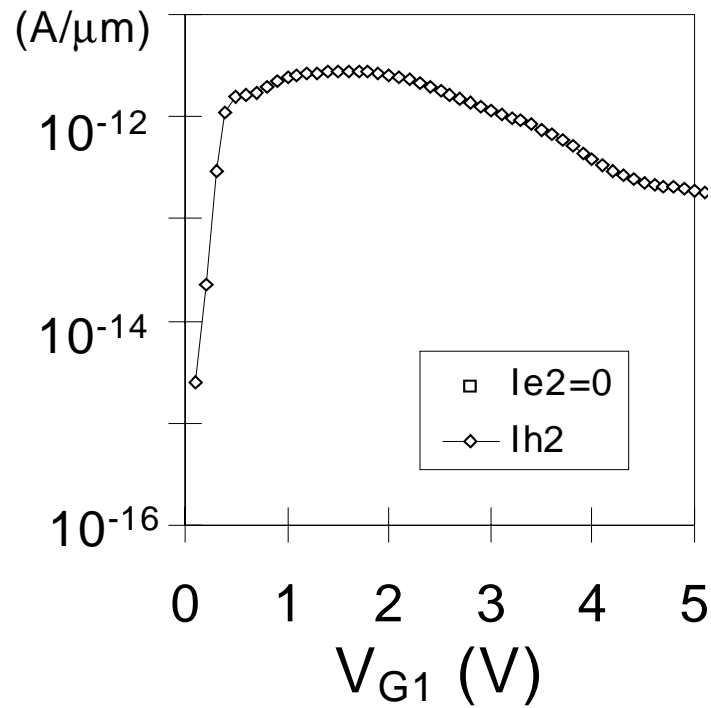
Methodology/ Characterization

- Experimentally
 - hot carrier stressing
 - substrate current (as a monitor of degradation) measurement
 - single transistor latch up voltage characterization
- By simulation
 - map:
 - electric potential
 - electric field,
 - current path,
 - calculate :
 - hot carrier generation
 - hot carrier injection current

1. OCBI Technique (Opposite Channel Based Injection)



Pure Hole Injection Into the BOX

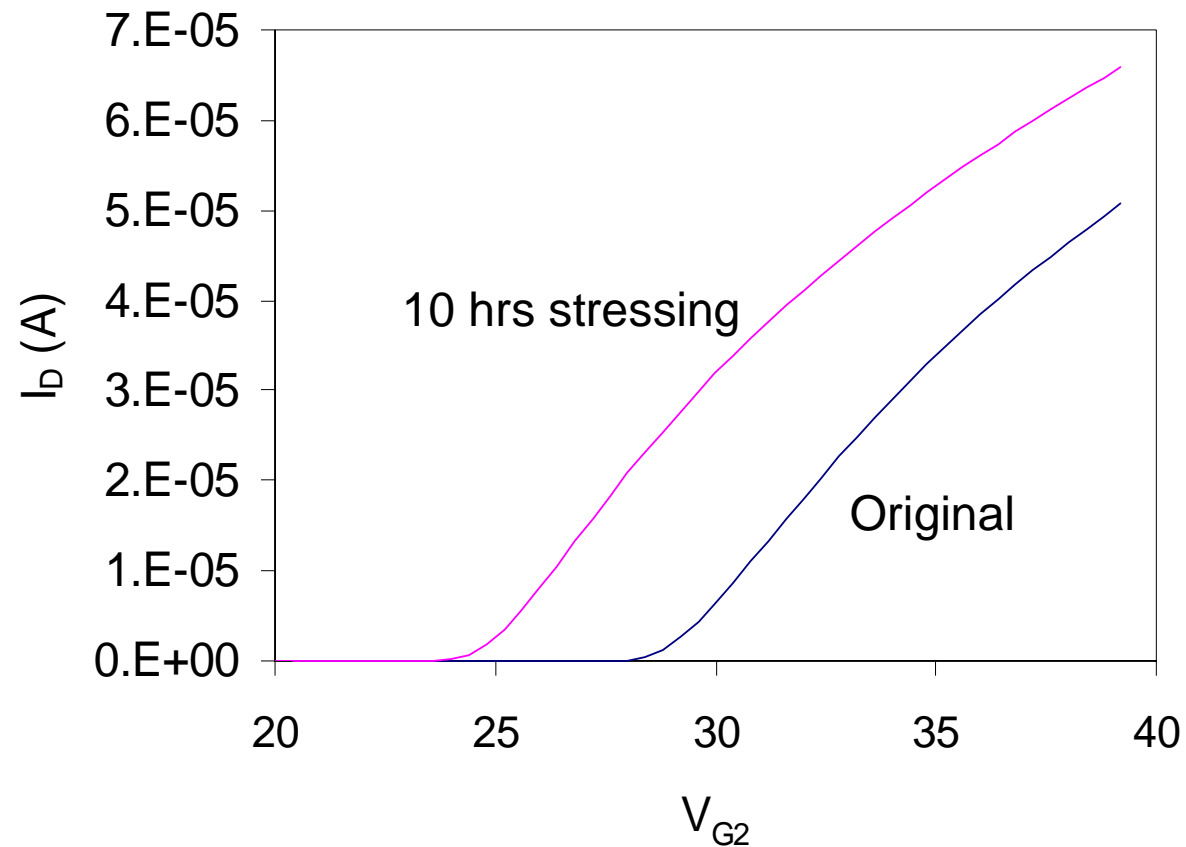


I_{h2} : hole injection current

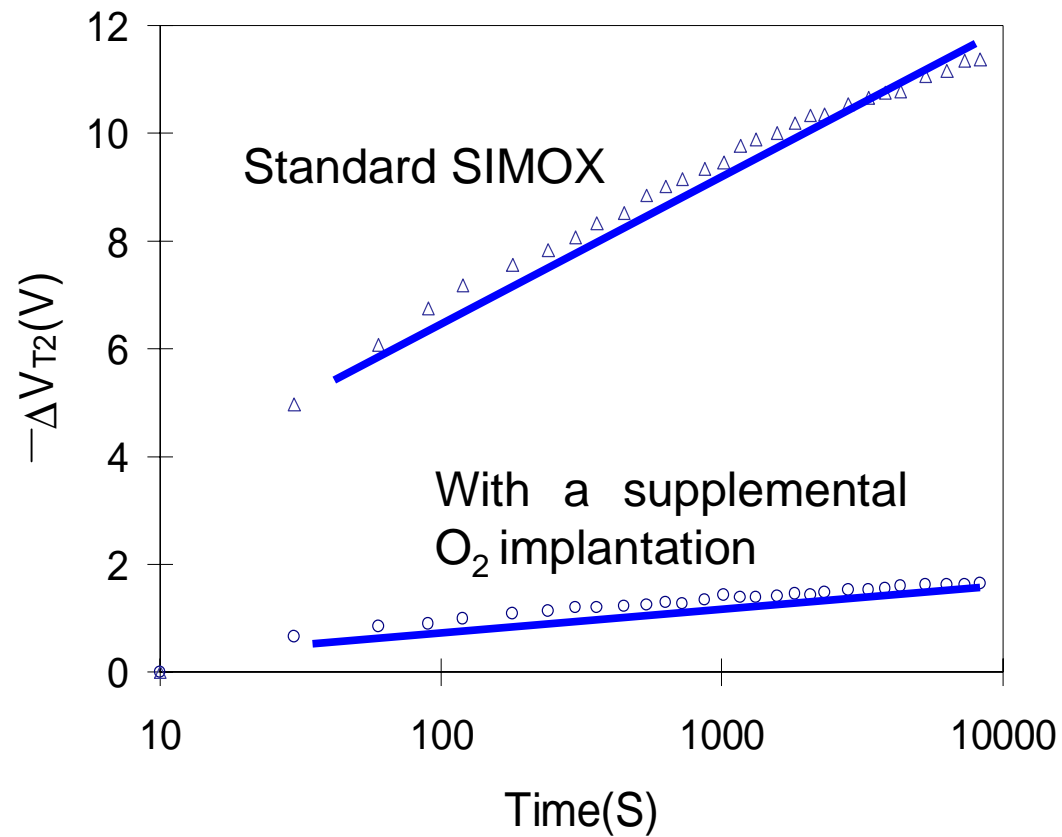
I_{e2} : electron injection current

$V_D=7V$, $V_{G2}= -30V$.

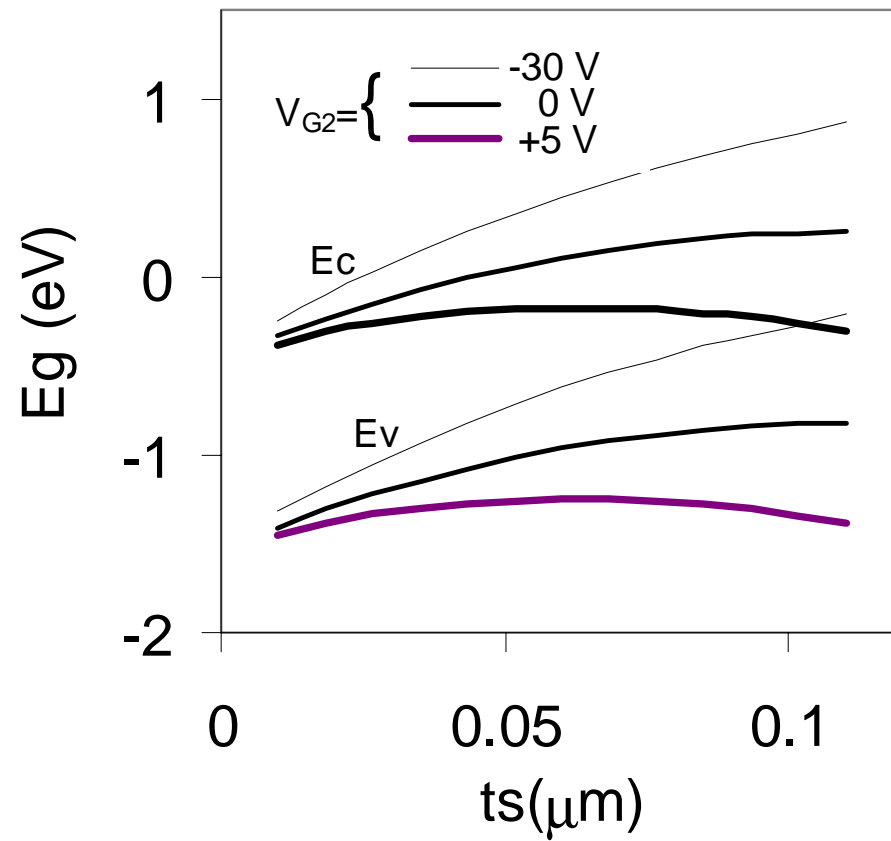
Shift of I_D - V_{G2} Characteristics After Hole Injection



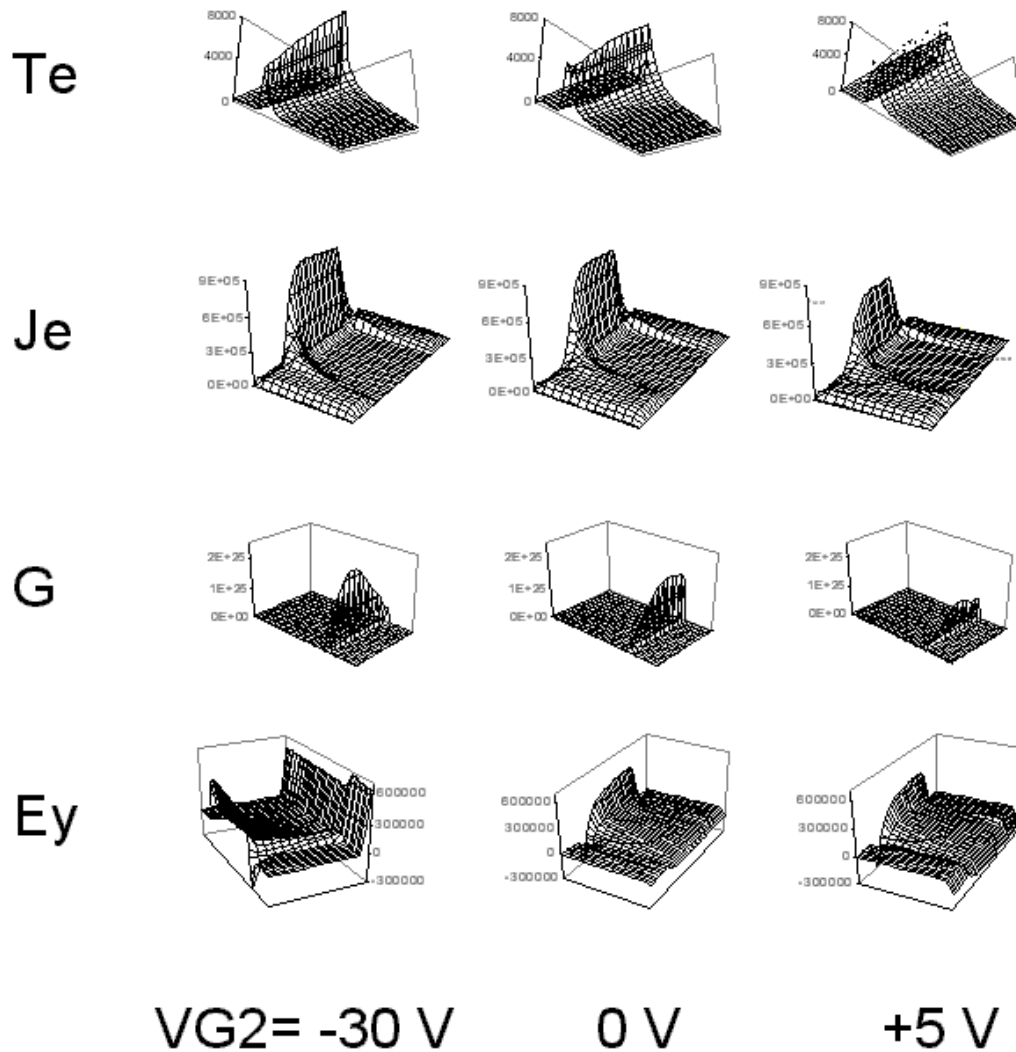
Back Threshold Voltage Shift ($-\Delta V_{T2}$) as a Function of Stress Time



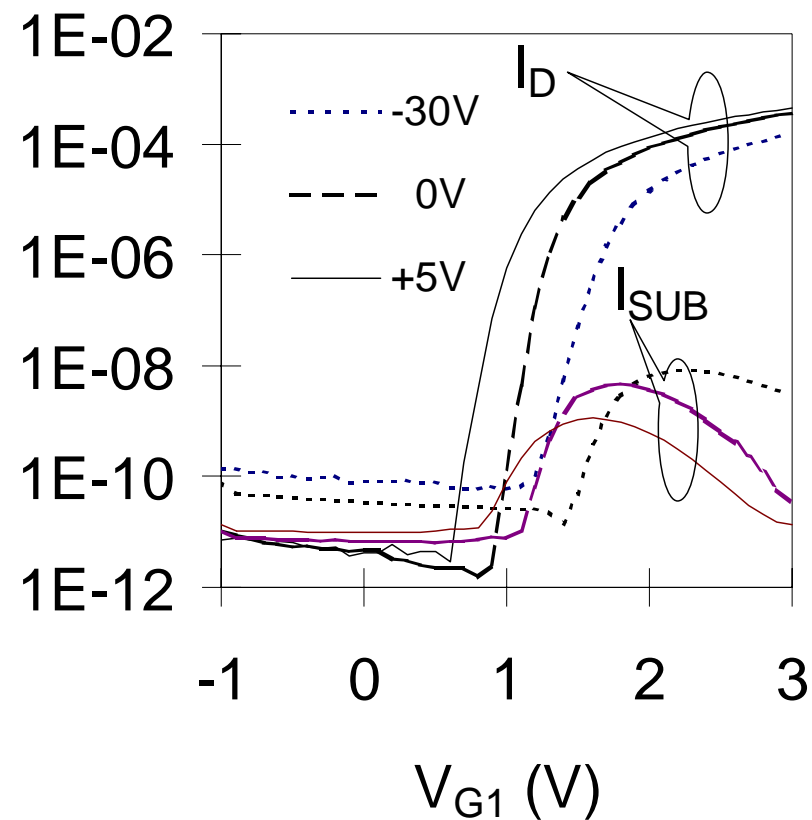
2. Channel Coupling



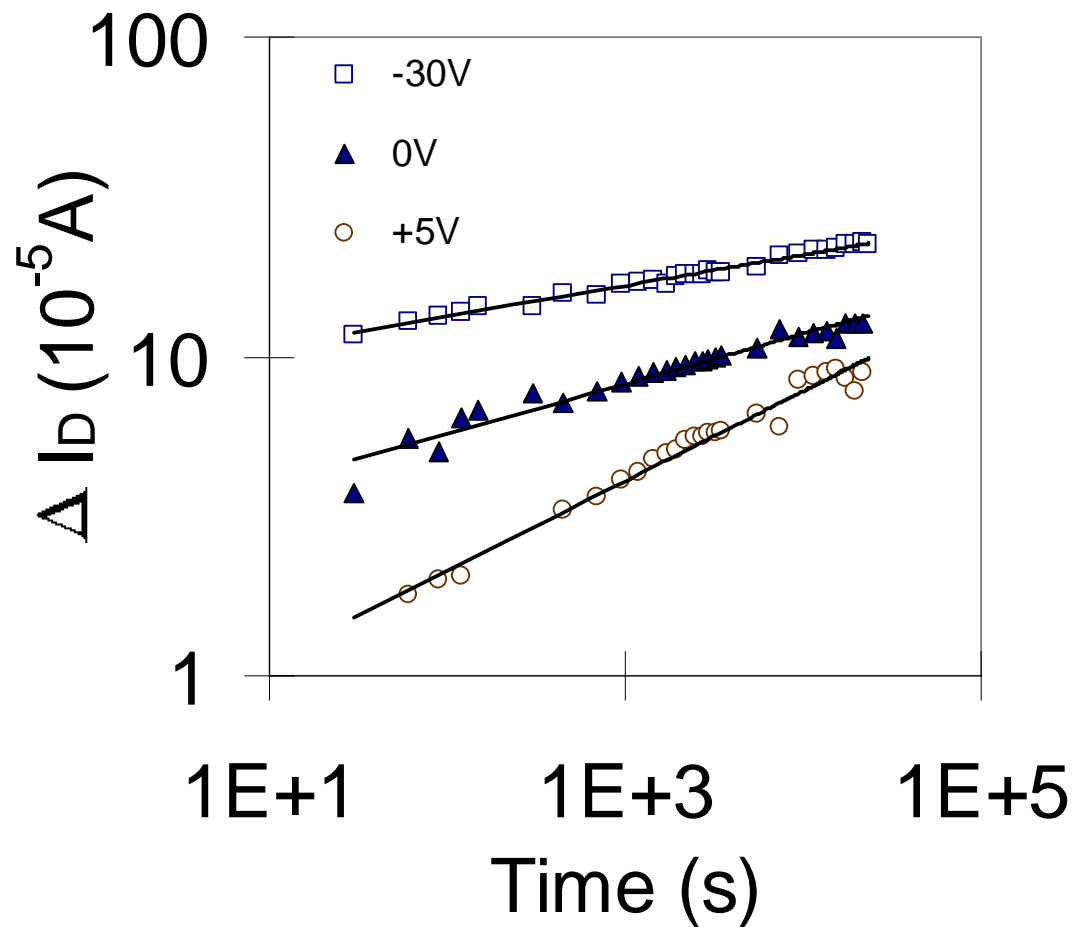
Channel Coupling Effect on Hot Carrier Temperature, Impact Generation and Electric Field



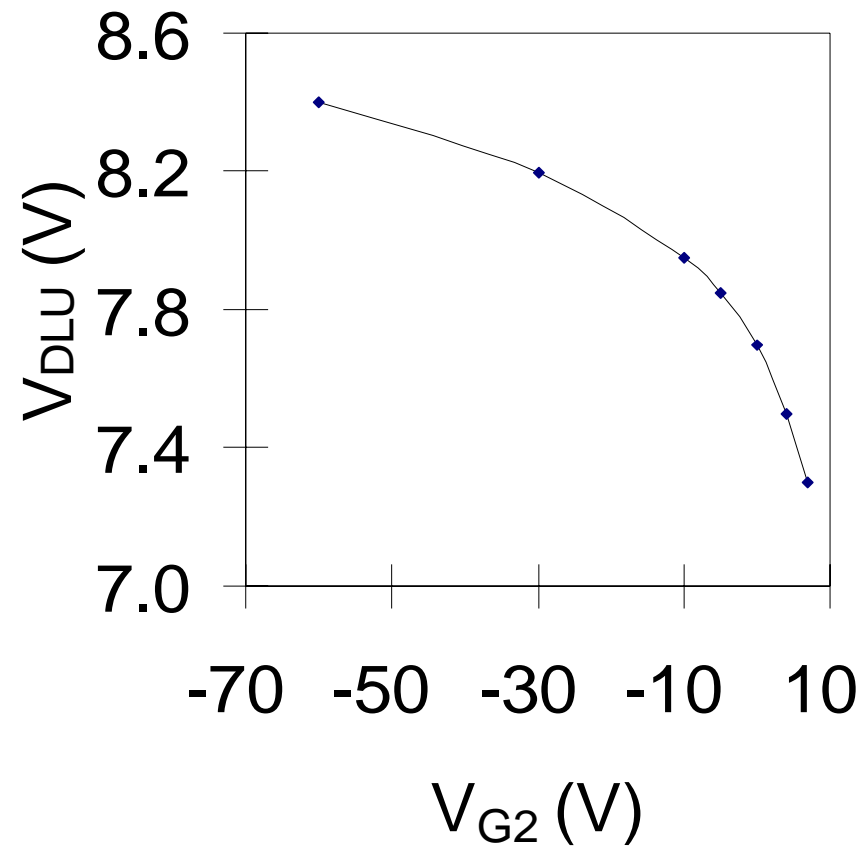
Substrate Current Dependence on the Back Gate Bias in FD SOI MOSFET



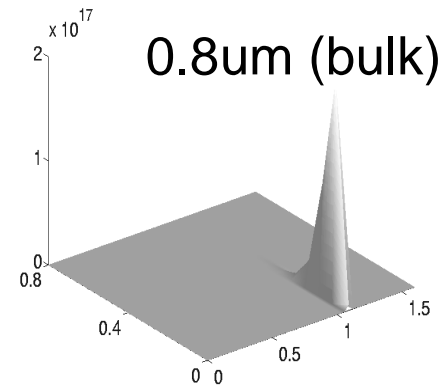
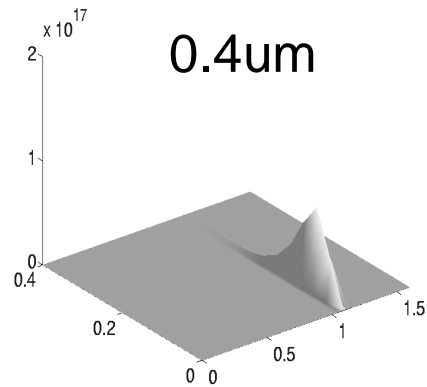
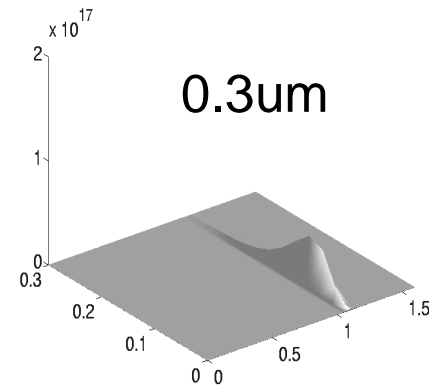
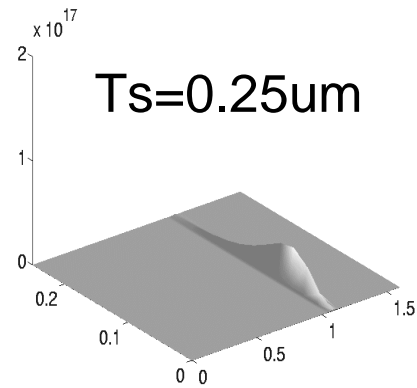
Channel Coupling Effect on Hot Carrier Degradation



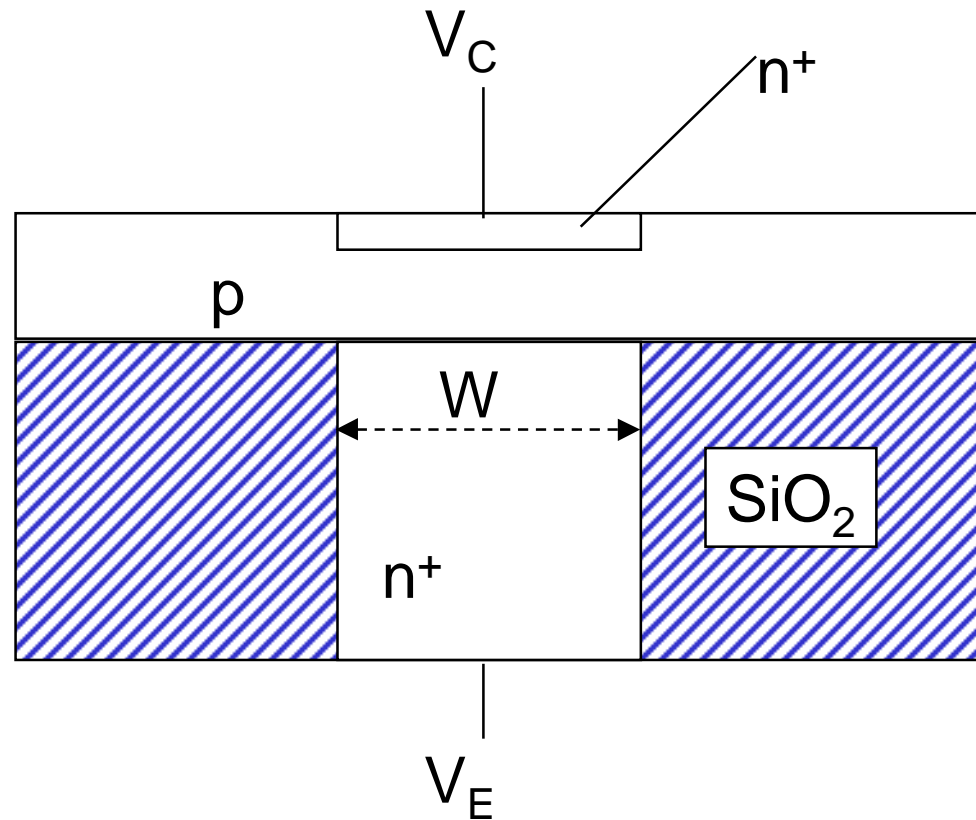
Channel Coupling Effect on Single Transistor Latch-up



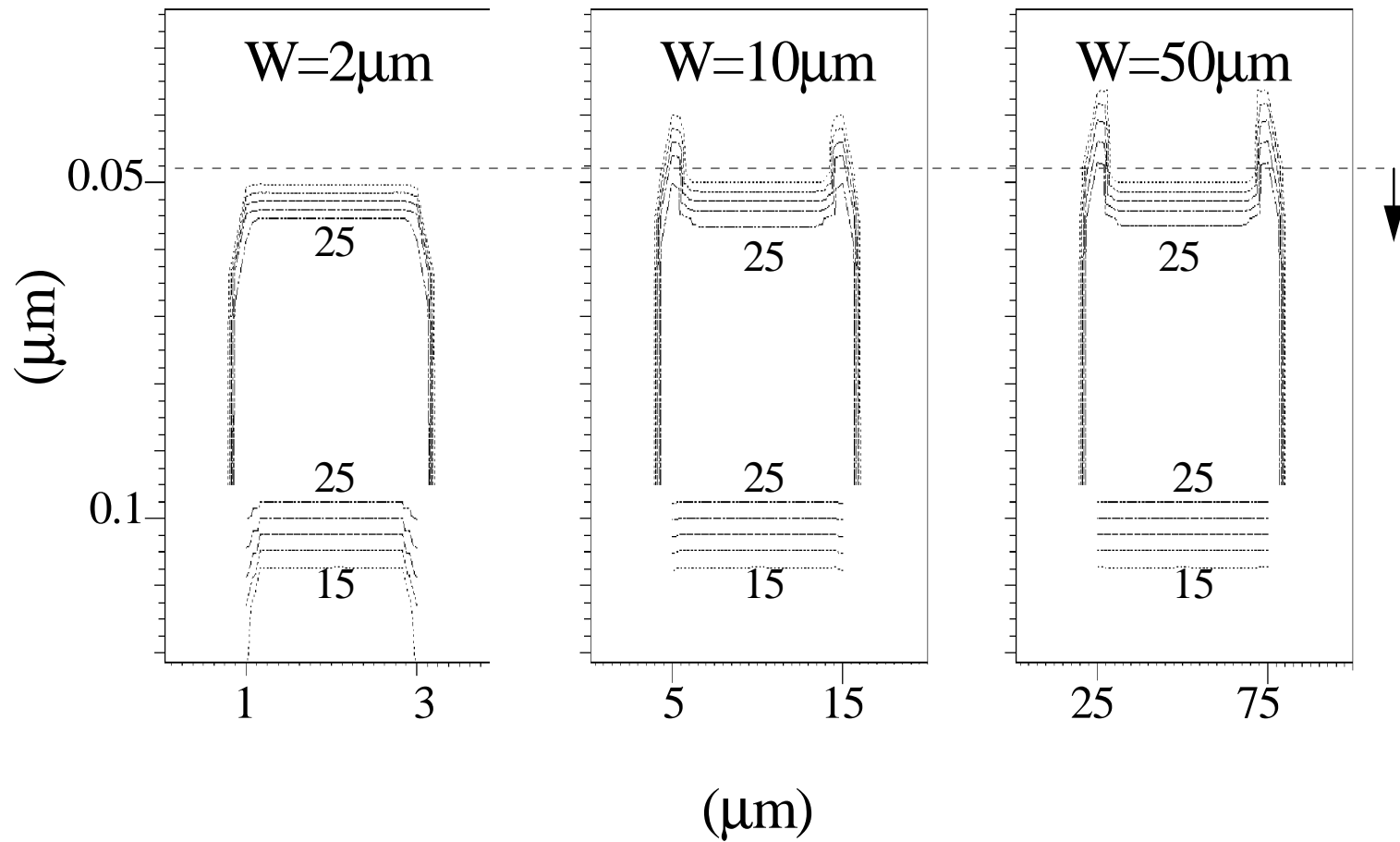
Impact Generation Rate as a Function of Silicon Film Thickness



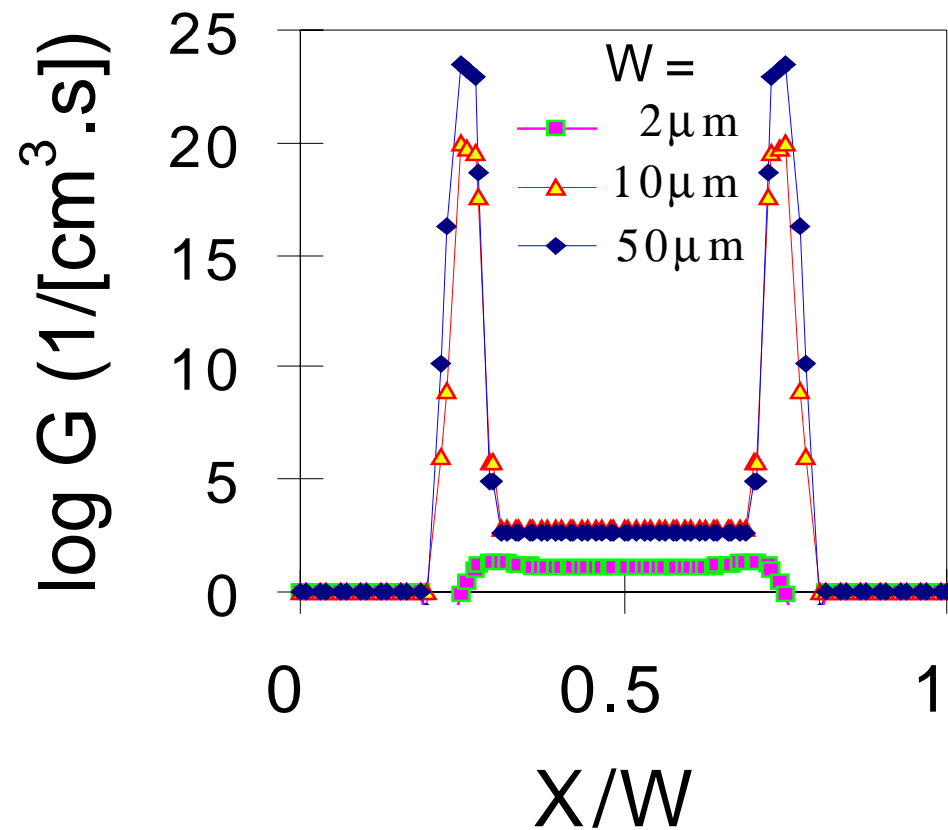
3. Study of Floating Body Effect (FBE) its Edge and Width Effect



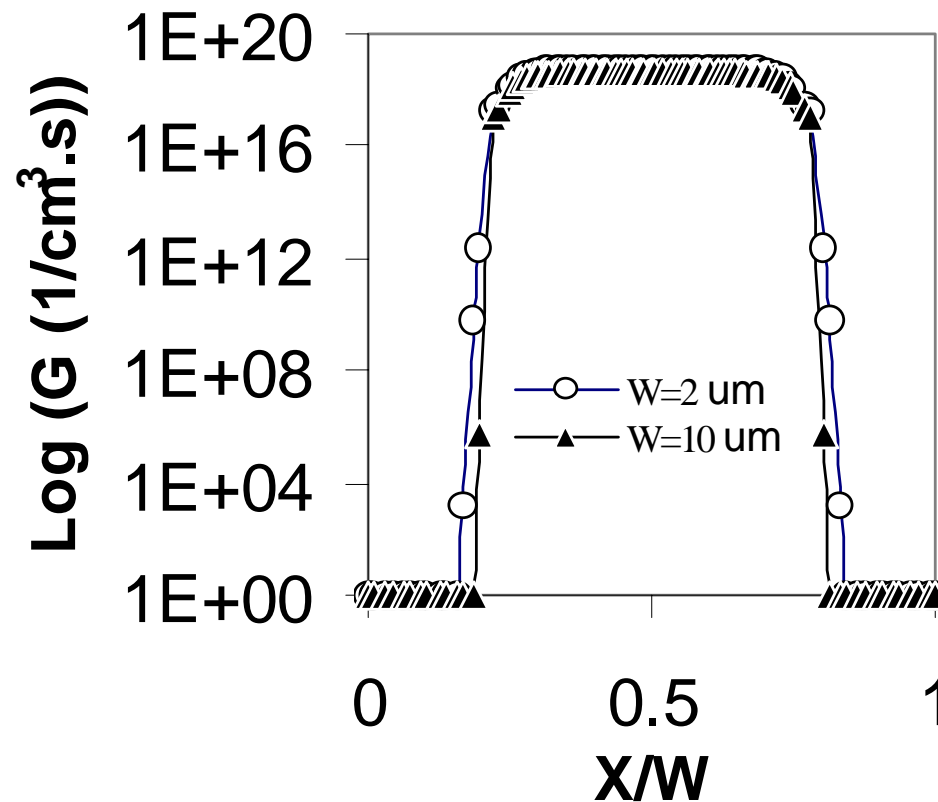
Contour Plot of Impact Generation Rate for Different Channel Width



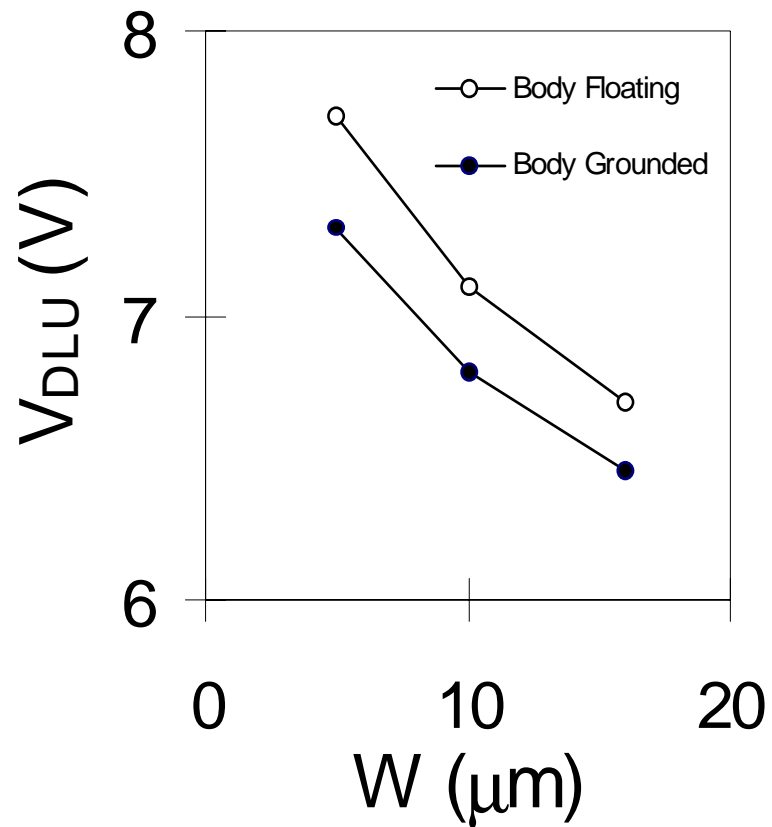
Abnormally Higher Impact Generation Rate at the Edges



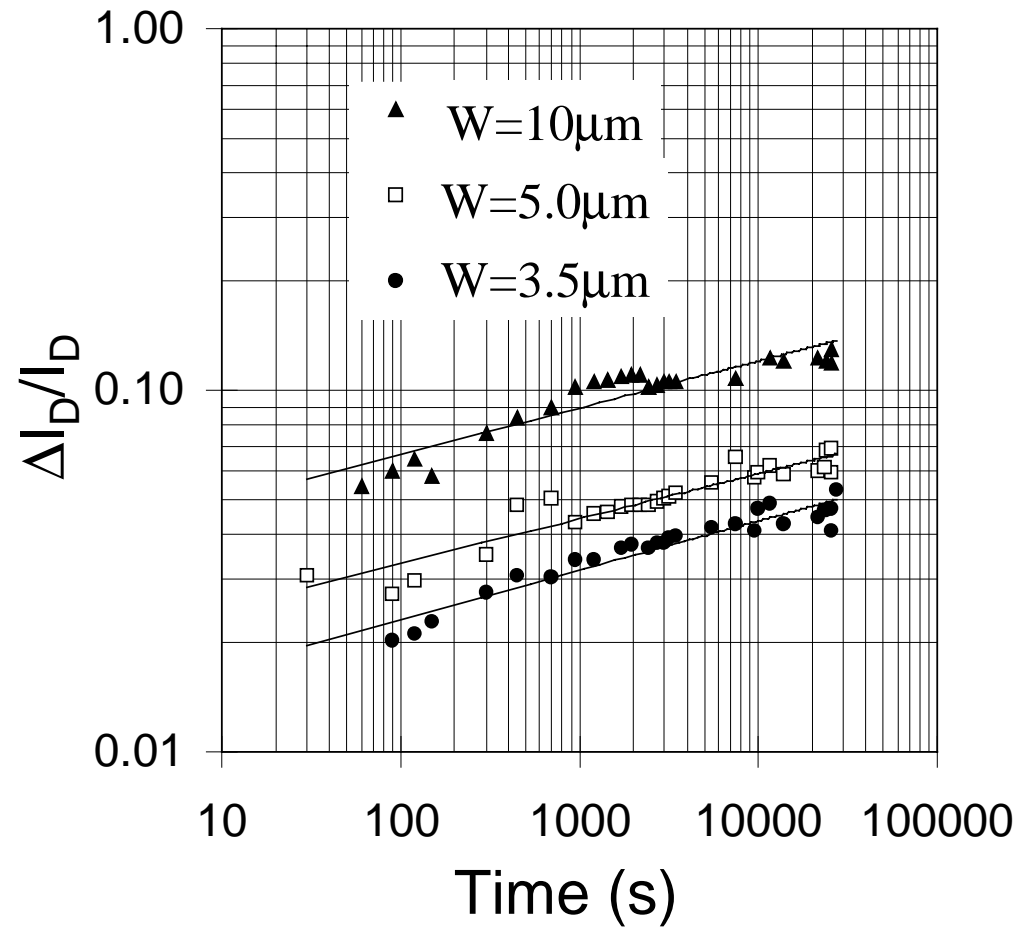
Impact Generation Rate at the Edges When the Body is Grounded



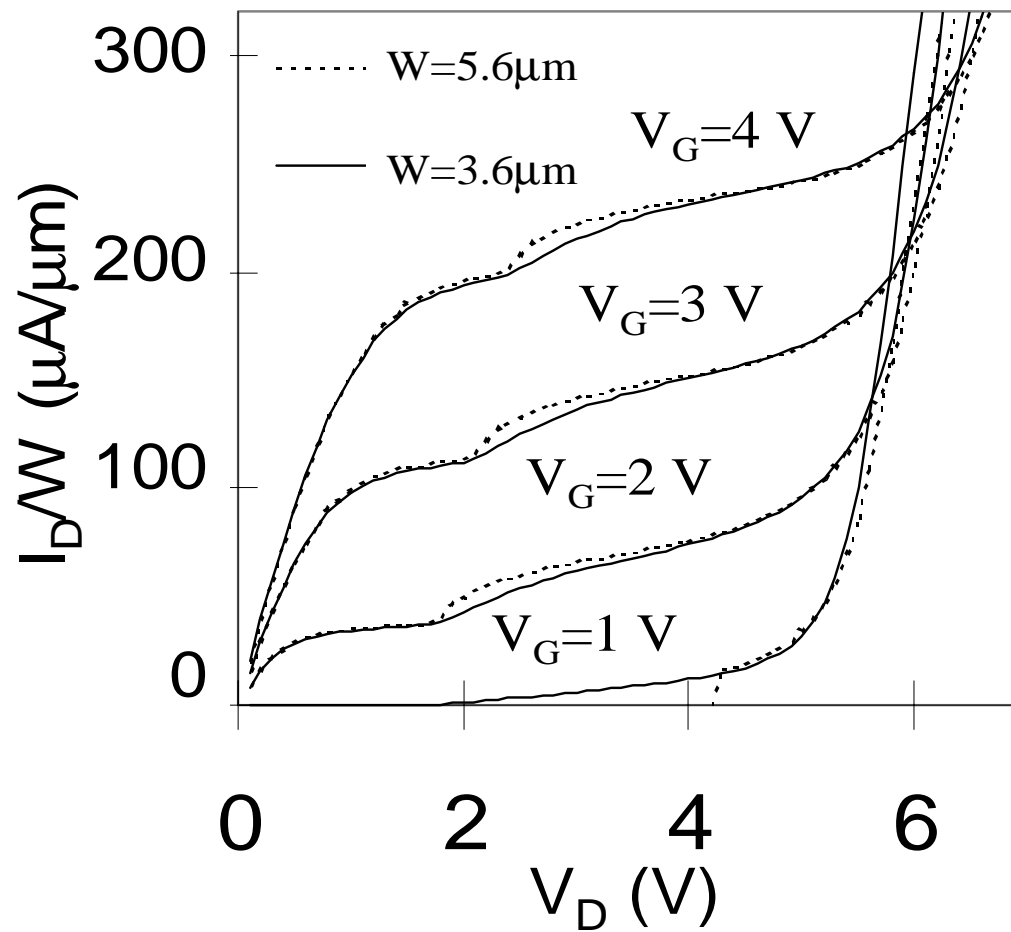
Single Transistor Latch-up Voltage as a Function of Device Width



Hot Carrier Degradation of Three Devices with Different Width

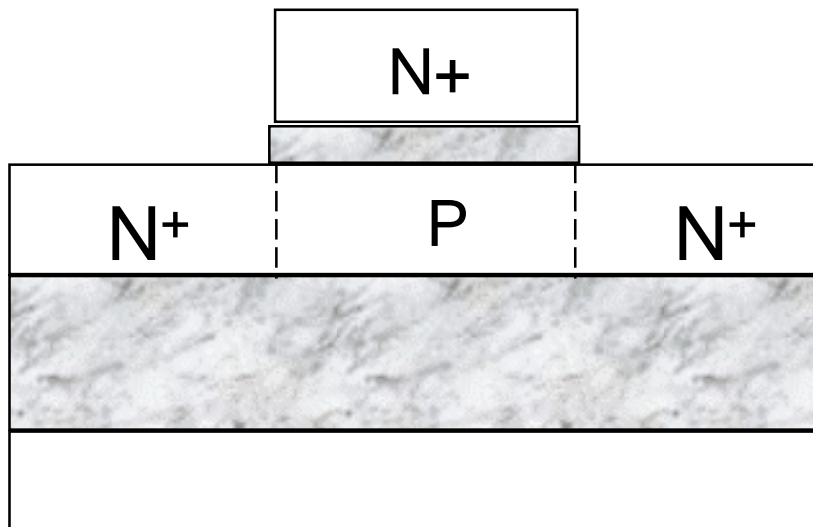


Kink Effect Dependence on Channel Width

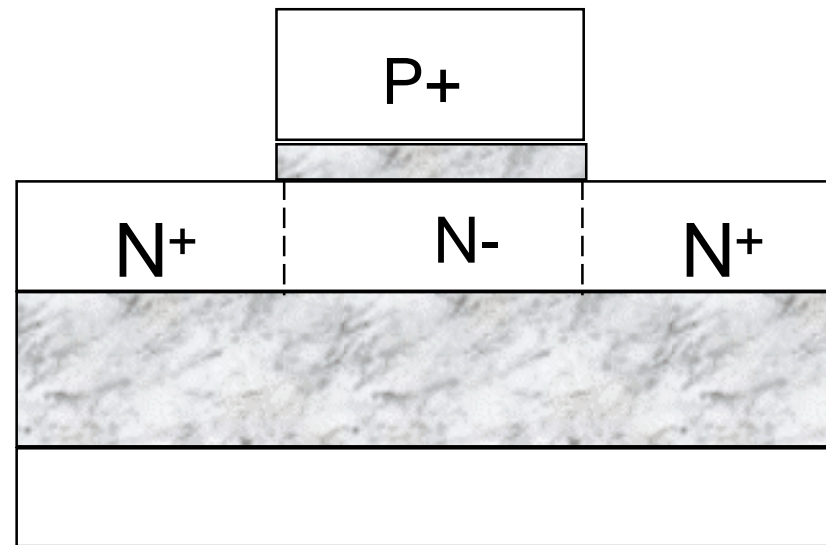


4. A New FD SOI MOSFET Structure

Two existing FD SOI MOSFETs

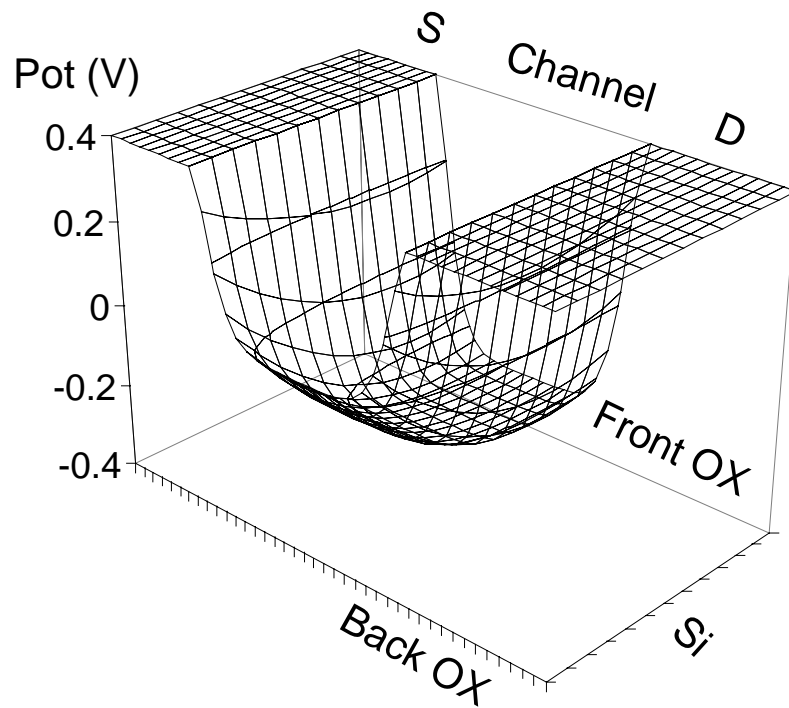


INV: inversion mode

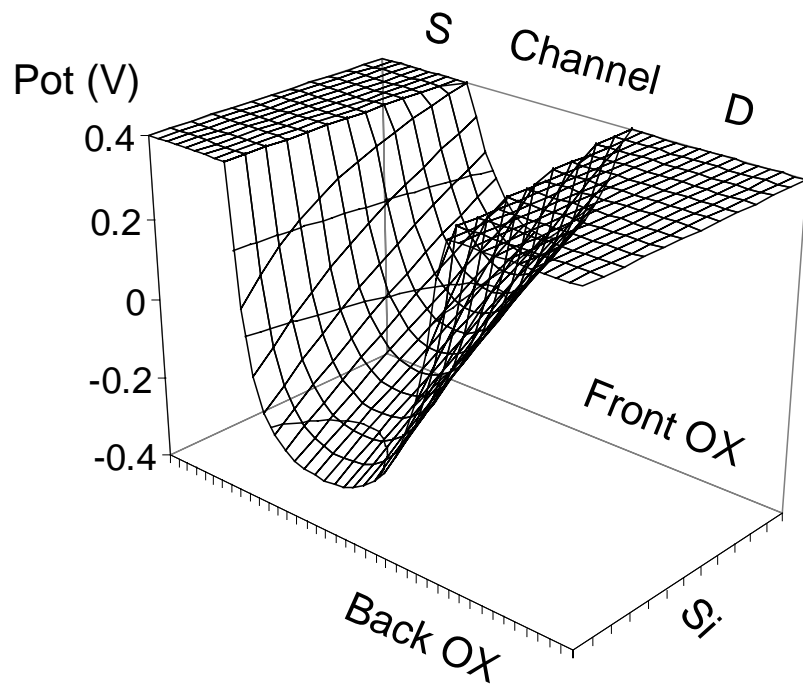


ACC: accumulation mode

Potential Profiles of the Inversion and Accumulation Mode FD SOI MOSFET

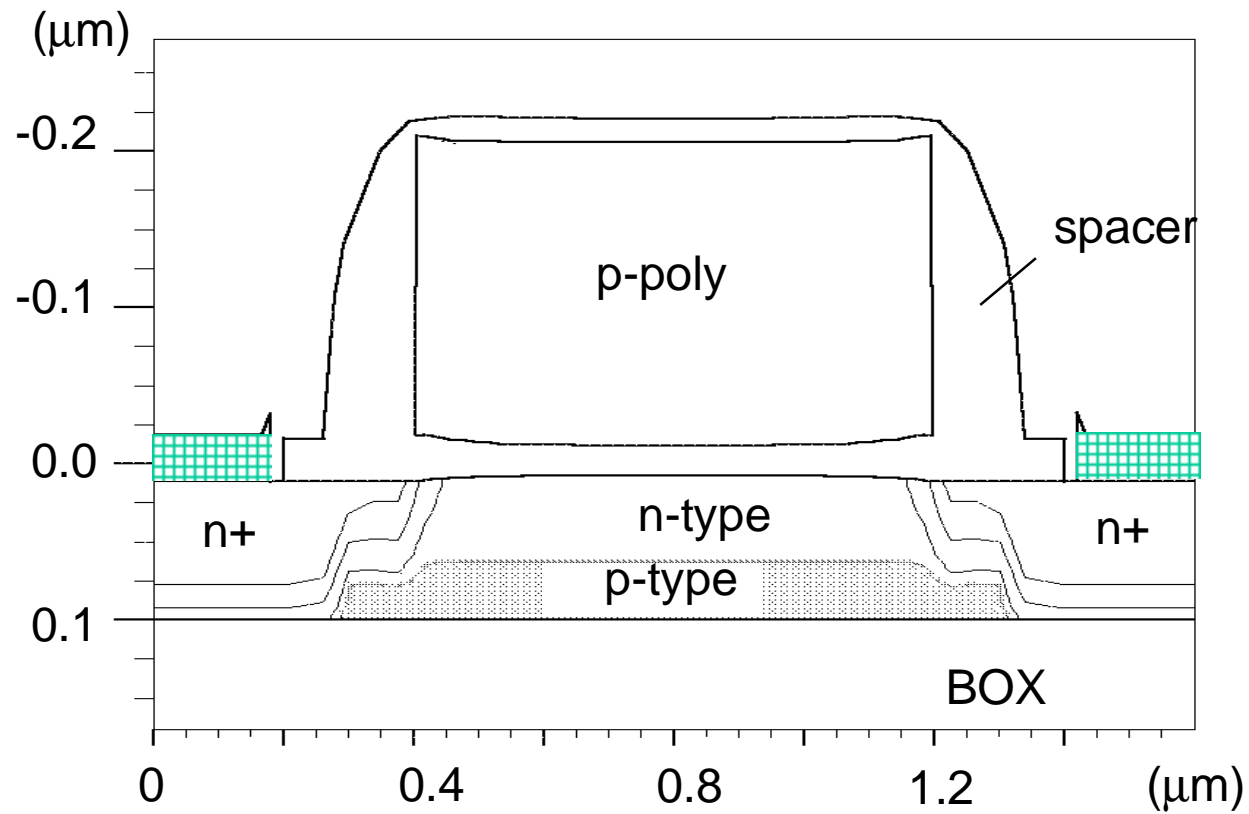


Inversion Mode

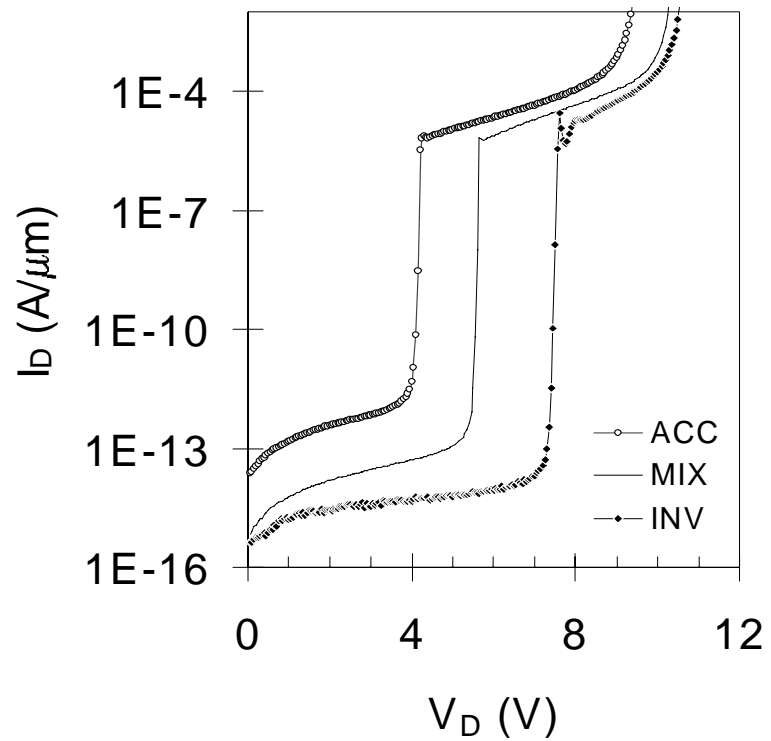
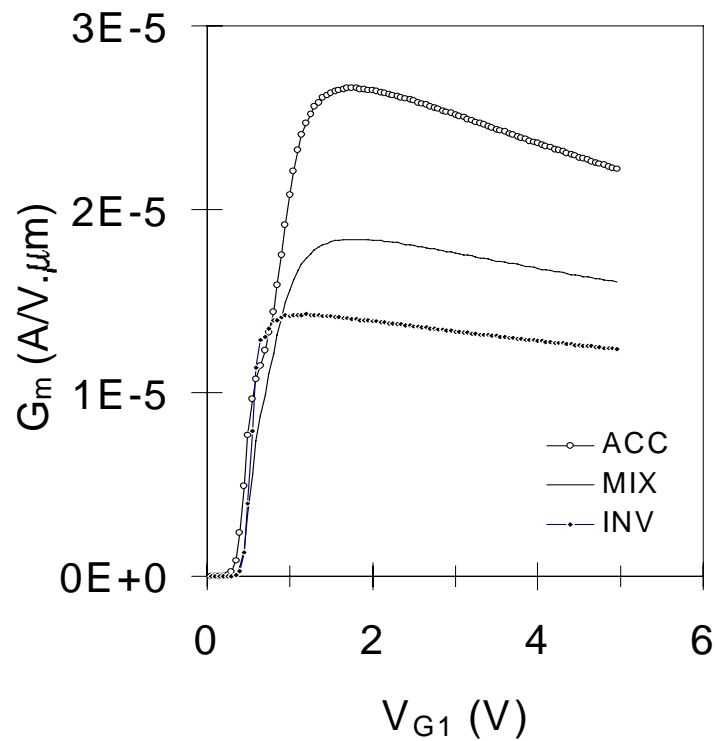


Accumulation Mode

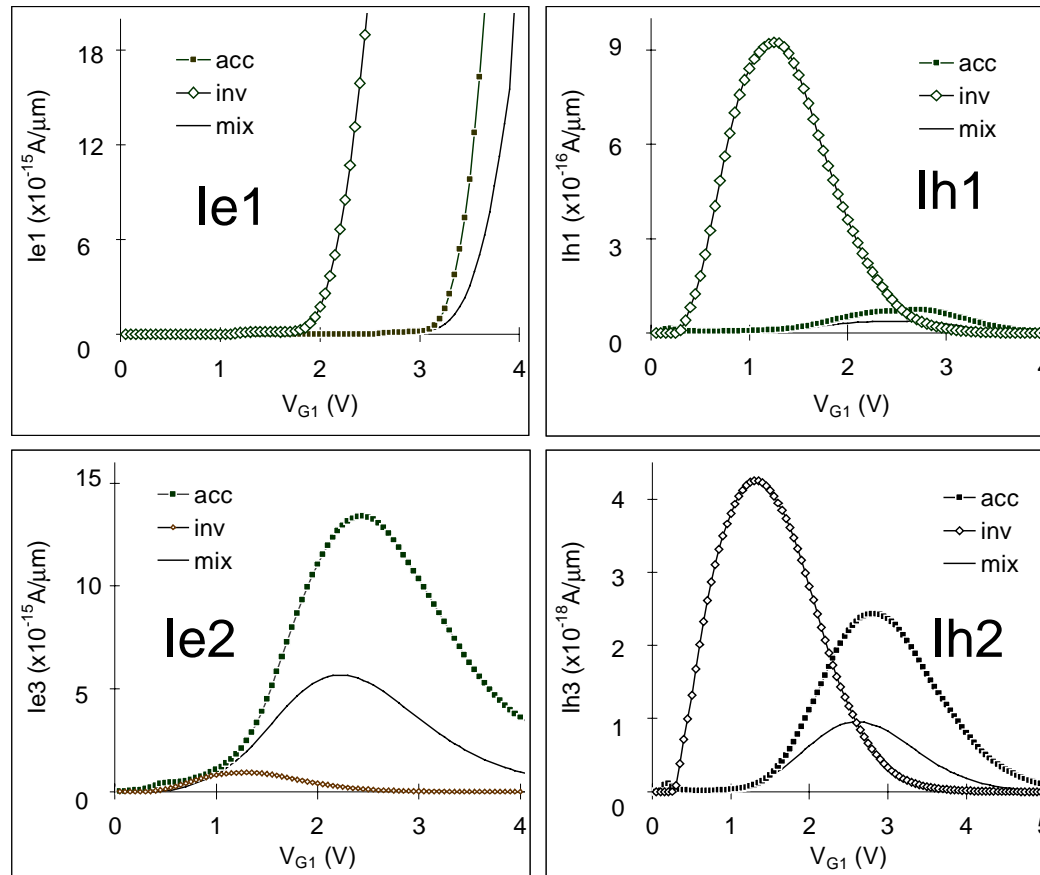
Virtually Fabricated New SOI Device (by SUPREM)



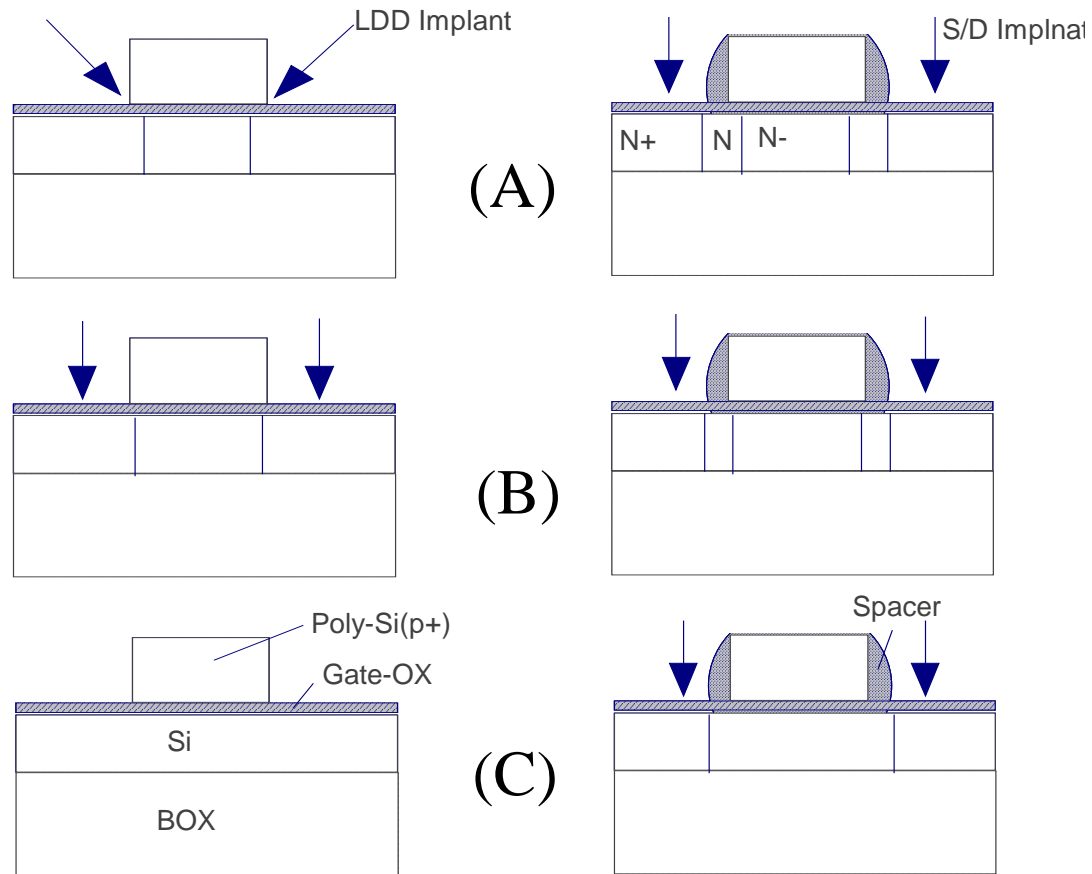
Comparison of Transconductance and Latch-up Voltage of the Three Devices



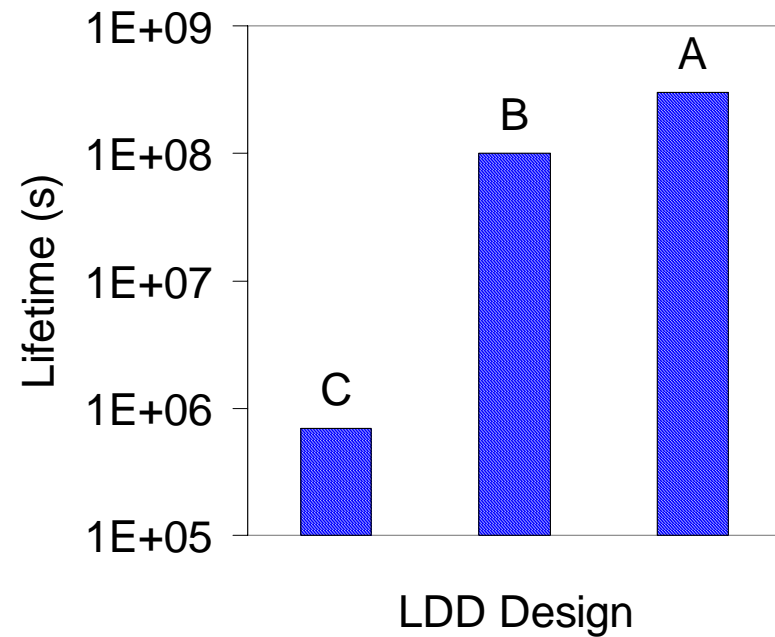
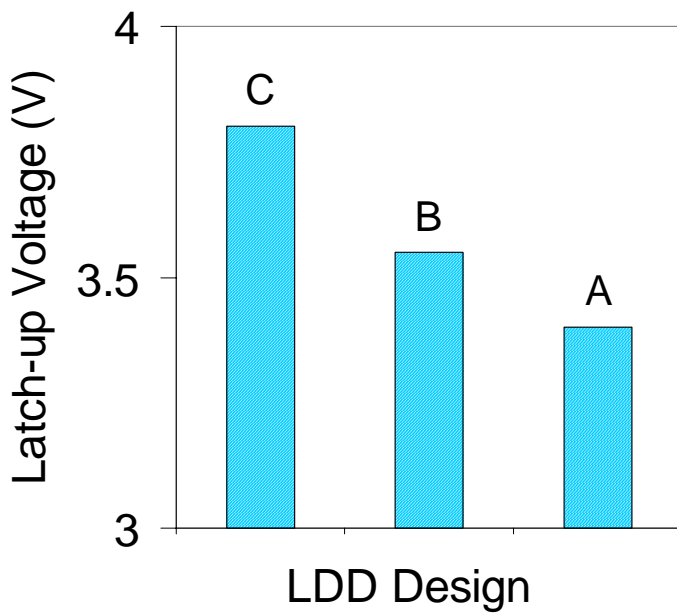
Comparison of the Hot Carrier Injection of the Three Devices



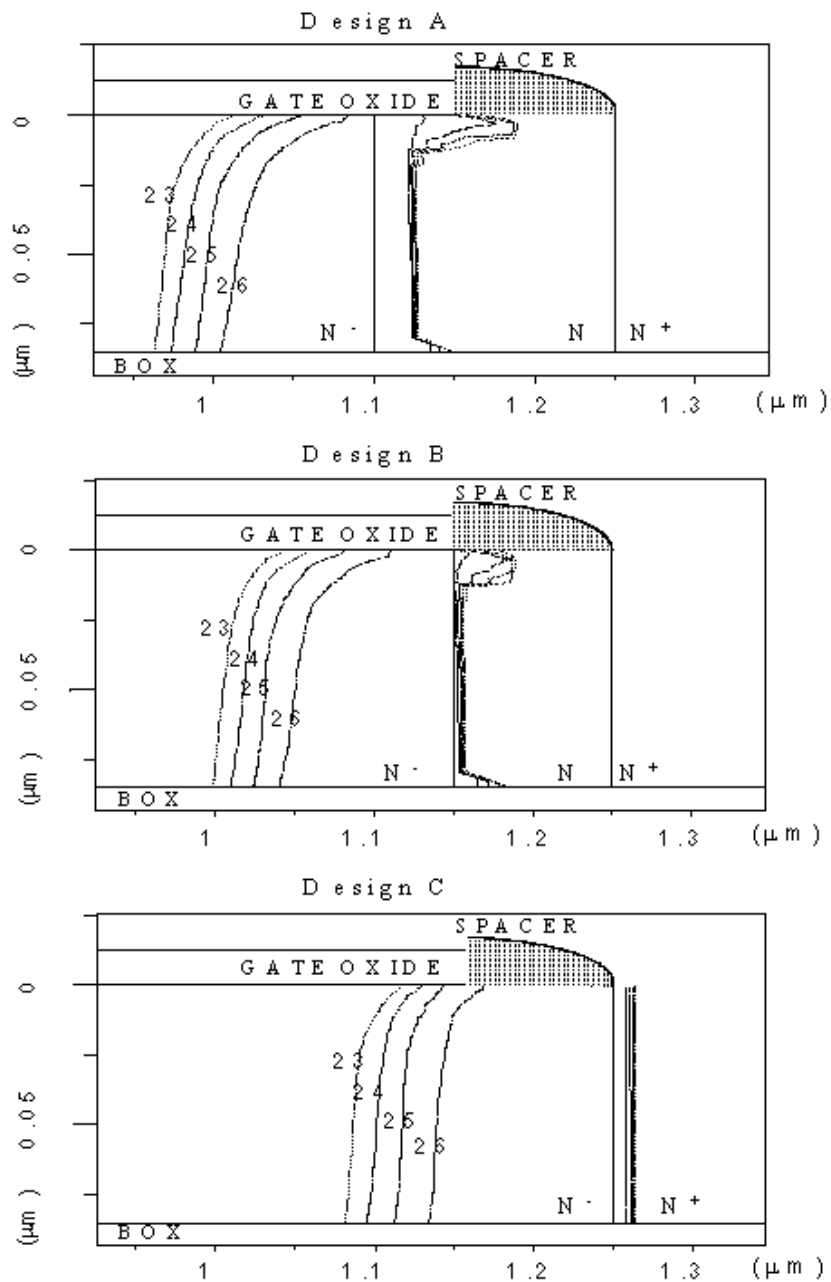
5. LDD Design Tradeoff in SOI MOSFET



Experimental Results: Tradeoff Between Performance and Reliability)



Contours of Impact Generation Rate of the Three LDD Designs



Comparison of Impact Generation Rate and Latch-up Voltage

Structure	Impact Rate Integral (1/cm ² s)				Latch-up Voltage (V)
	Top	Middle	Bottom	Average	
A	8.5x10 ²⁰	1.7x10 ²²	2.9x10 ²²	1.6x10 ²²	3.40
B	8.0x10 ²⁰	8.2x10 ²¹	2.3x10 ²²	1.1x10 ²²	3.55
C	7.9x10 ²⁰	1.5x10 ²¹	1.8x10 ²¹	1.4x10 ²¹	3.80

Summary of the Results

- Opposite channel based injection can happen by the aid of dual gate control and this phenomenon can be used as a tool to study the hot carrier degradation
- Channel coupling imposes a trade-off between the hot carrier reliability and single transistor latch-up in SOI MOSFET
- The rate of carrier generation rate is higher at the edge of SOI MOSFET and more so for wider devices. Wider devices have lower breakdown voltages.
- A new structure was proposed which holds the weaknesses of the current FD SOI MOSFETs and is more resistant to hot carrier injections
- Optimized bulk LDD technology faces a tradeoff between hot carrier reliability and single transistor latch-up in SOI MOSFET