6. LDD Design Tradeoffs on Latch-Up and Degradation in SOI MOSFET

An experimental study has been conducted on the design of fully depleted accumulation mode SOI (SIMOX) MOSFET with regard to hot carrier reliability, single transistor latch-up and device performance. Three drain designs were considered, using LArge Tilt-angle Implanted Drain (LATID) for the LDD formation. Structures incorporating zero-degree-angle LDD implant, large-angle LDD implant, and no LDD were fabricated, and their hot carrier reliability, single transistor latch-up voltage and device performance in terms of drive current and speed were examined. Correct interpretation of the experimental results was aided by performing PISCES numerical simulations. It was found that the structure with the best hot carrier reliability (large angle LDD implant) has the worst latch-up voltage, and the one with the worst hot carrier reliability (no LDD implant) has the best latch-up voltage. Overall device performance with acceptable hot carrier reliability and latch-up voltage is obtained with the 0°-angle LDD implant.

6.1 Review of Previous Works

The LDD (Lightly Doped Drain) in MOSFET was first proposed in late 1970's to elevate the hot electron injection problem in scaled MOSFET [1]. As seen in Figure 6.1 (a), an extra low doped n- offset region is inserted between the channel and drain as compared to the conventional device. This lightly doped buffer smoothes the abrupt drain junction and yields a lower electric field near the drain (b). Reducing the electric field is a very effective way to solve all the hot-carrier related problems and LDD technology since then has been widely used in VLSI production [2].

Following bulk technology practice, most of the research and development efforts to date have been directed towards enhancement mode devices. Because of the very thin silicon films involved, these devices require high doping concentrations in order to obtain useful threshold voltage values, leading to substantial mobility degradation. Since accumulation mode devices do not suffer from this problem, there has recently been a considerable effort to explore them as a viable alternative to enhancement mode technology [68-72]. It must be noted, however, that accumulation mode devices are not free from FBE (such as early breakdown and single transistor latch-up) as it might at first be expected [8], which are better known to occur in enhancement mode devices. In addition, as device dimensions and film thickness continue to shrink, there are increased concerns regarding the hot carrier reliability of SOI technologies (both for enhancement and accumulation mode) [9] [10].

Based on the experience gained from bulk silicon technologies [11], suitable LDD drain engineering approaches are been currently investigated to achieve hot carrier resistant SOI structure [72]. At the same time, it has been recognized that correct drain engineering can also be used to control problems arising from the floating body [28]. An interesting drain engineering approach, the so-called large-tilt-angle implanted drain (LATID) [12] [13] has been recently applied successfully to the enhancement mode FD SOI transistors [14]. The purpose of this chapter is to investigate the application of LATID to accumulation mode SOI MOSFET, and discuss its impact on hot carrier degradation and single transistor latch-up control. This will establish the corresponding device design tradeoffs, and will ultimately lead to the devices of good performance with acceptable levels of both hot carrier reliability and breakdown voltages.

6.2 Experimental Details

In the approach taken in this work, devices identical other than LDD design were measured for hot carrier degradation and single transistor latch-up, and PISCES simulations [47] were carried out for the correct interpretation of the experimental results. The devices were fabricated in the Lockheed Martin Federal Systems SOI (SIMOX) 0.5 μm CMOS accumulation mode technology, using reverse type gates (n^+-poly for p-channel, p^+-poly for n-channel) [68] [69]. In our work, n-channel transistors were studied with gate oxide, silicon film and buried oxide thickness equal to t_{ox1}=12.5nm, t_{Si}=85nm, and t_{ox2}=400nm, respectively, and silicon film doping of about $3x10^{16}$ cm^{-3}. The devices have the same drawn gate length (L_G=0.7μm) and spacer width (0.1μm), but different effective channel lengths

due to the different drain implant processes. As shown in Figure 6.2, the LDD implant was performed at a large tilt angle (A), or perpendicularly (B). For comparison, devices without LDD implant were also fabricated (C). From SUPREM process simulations it is fairly accurate to assume LDD doping of $3x10^{18}cm^{-3}$, and LDD length of 0.15µm, 0.1µm and 0.0µm from the outside edge of the spacer for designs "A", "B", and "C" respectively. These correspond to effective channel lengths of 0.6µm for "A", 0.7µm for "B", and 0.9µm for "C". For studying the hot carrier reliability, the devices were stressed for 8000 sec at a front gate voltage equal to one half of the drain voltage for three different drain voltage values: 3.2V, 3.4V and 3.6V (all below avalanche breakdown voltage measured to be larger than 4.0 V [64, Fig.1]). During the stressing, the back gate was kept grounded. It should be noted here that although the worst case of degradation for SOI transistors usually occurs for gate voltage close to the threshold voltage ($V_{G1} = V_{T1}$) [64] [72] [73], for the present devices the degradation does not depend as strongly on gate bias [64, Fig.2].

The hot carrier induced degradation of both the gate and buried oxides were examined by basic static-transistor-characteristic measurement [72]. The single transistor latch-up voltage is determined by I_D-V_{G1} characteristics with different drain voltages (ref Figure 3.3).

6.3 Results and Discussions

Prior to hot carrier stress, both the gate and buried oxides were examined for basic integrity via step-and-hold high field stress. It was found that the gate oxide reached 100%

cumulative failure at an electric field of 9.5 MV/cm, while the buried oxide reached 100% cumulative failure at 6 MV/cm. The relatively low breakdown field for the gate oxide is attributable in part to the device test set-up. Since fully depleted devices were used, the breakdown tests were done by applying a bias to the gate with the body grounded through the source and drain. Therefore, it is likely that edge effects reduced the breakdown voltage. The low breakdown field obtained for the buried oxide are in line with previously reported results for SIMOX buried oxides [15] [16], and have been attributed to a silicon-rich region around the top of the oxide [79].

Several trends emerged from the hot carrier testing: Within the bias range studied, the hot carrier degradation was essentially independent of the stress bias. Although this might seem a little surprising at first, it is expected considering that the devices are operated during stress below avalanche breakdown [64, Fig.1]. The largest back-channel threshold voltage shifts (ΔV_{T2}) seen were around 0.2 V, too low to influence significantly the front channel through electrostatic coupling [45]. Finally, the degradation manifested itself as loss in drive current and transconductance rather than threshold voltage shifts, for both (front and back) channels. Table 6.1 shows the measured transconductance degradation of the front and the back channel and the corresponding hot carrier lifetime (defined as the stressing time required to cause a 10% reduction in the drive current) for all three LDD designs. It is seen that design "A" sustains the minimum transconductance degradation and design "C" the maximum. It is also seen that in accordance with the transconductance degradation results, design "A" has the longest lifetime and design "C" the shortest: $3x10^8$s, $1x10^8$s, and $7x10^5$s for design "A", "B", and "C", respectively. Table 6.1 also summarizes the results of the

single transistor latch-up measurements, which show the LDD "A" design results in the lowest latch-up voltage and the "C" to the highest: V_{DLU}=3.40V, 3.55V, and 3.80V for design "A", "B", and "C", respectively.

By comparing the results above, it quickly becomes apparent that the design with best hot carrier performance ("A") exhibits the poorest single transistor latch behavior and vice versa, i.e. design "C" has the largest latch-up voltage but the worst hot carrier reliability. Based on these results, design "B" must be chosen for good overall hot carrier reliability and single transistor latch-up behavior. To get a better feel of the factors at play that underlie this tradeoff and provide insight for further device optimization, the devices were simulated under the hot-carrier-stress condition (V_{G1}=1.6V, V_D=3.2V, back gate grounded) to examine the carrier impact generation rate G profile within the device structure. Again, for added accuracy, the calculations were done self-consistently, by keeping the impact ionization switched on during the simulations. The results for the three structures are shown in Figure 6.3, where the generation rate contours are plotted in the silicon film region near the drain. It is seen that contour of maximum carrier generation ($10^{26}cm^{-3}s^{-1}$) in the channel is entirely under the gate for device "A", shifts towards under the spacer for device "B", and is completely under the spacer layer for device "C". Combining this observation with the fact that the spacer is usually more susceptible to hot carrier degradation, it can now be seen that design "A" should have the best hot carrier reliability because the majority of impact ionization carriers are generated at a "safer" area away from the spacer. The majority of impact ionized carriers in design "C", on the other hand, are generated very close to and under the spacer, resulting in the worst hot carrier reliability devices.

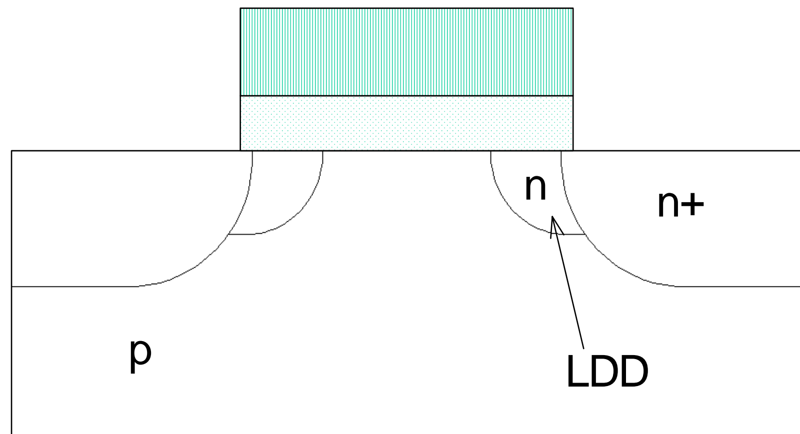
In order to get more insight on the single transistor latch-up from the above simulations, an estimate of the total impact ionization carrier generation was obtained by suitable integration, as shown in Table 6.2. The integration was made along three horizontal lines cut in the silicon film from source to drain: near the front, middle, and the back channel. It is found that the overall impact ionization is slightly larger in "A" as compared "B", and the smallest in "C". For reference, the values of the latch-up voltages (from Table 6.1) are also shown in Table 6.2. It is quite clear from that the amounts of total carrier generation in the various designs are in agreement with the observed latch-up voltages. The total impact generation was similarly estimated under the bias conditions that device "A" just latches up but devices "B" and "C" have not, i.e. at V_{G1}=0V and V_D=3.4V while V_{G1} was scanned in the positive to negative direction. The averaged values obtained were $2.17\text{x}10^{19}cm^{-2}s^{-1}$, $8.47\text{x}10^{12}cm^{-2}s^{-1}$ and $1.78\text{x}10^{12}cm^{-2}s^{-1}$ for design "A", "B", and "C" respectively, and they again agree well with the breakdown voltages.

In discussing the hot carrier reliability vs. single transistor latch-up tradeoffs as a function of drain design, one must also consider the effects that the drain design has on the device performance in terms of drive current and speed. The drive current was measured on unstressed devices at V_G=V_D=3.3V for all three drain designs, and the results are shown in Figure 6.4, which also shows the corresponding latch-up voltages

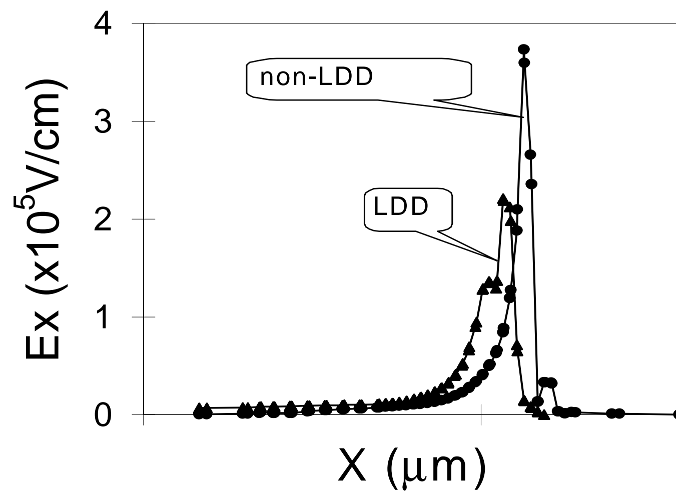
and hot carrier lifetimes for a reference. It is seen that one does not necessarily need to trade-off hot carrier resistance to maximize transistor drive current. However, one does need to trade it off against latch-up voltage. Finally, ring oscillators were fabricated with type "A", "B", and "C" devices but otherwise identical and their speed measured at 3.3V is shown in Table 6.1 for comparison. It is seen that maximum speed of operation of the ring oscillator is obtained at the expense of considerable reduction of the operating voltage margin.

6.4 Conclusions

The above results clearly demonstrate that there is a tradeoff between hot carrier reliability and latch-up voltage in optimizing the LDD structure for SOI MOSFET. For the drain engineering splits examined in this chapter, it was seen that improving the transistor latch-up voltage resulted in an increase in hot carrier degradation, and vice-versa, i.e. improving the hot carrier reliability resulted in a decrease of the latch-up voltage. With the help of PISCES simulation, this tradeoff can be explained by examining both the amounts of impact ionization rates and their positions relative to the spacer. Good overall device performance with acceptable hot carrier reliability and latch-up voltage is obtained with the 0°-angle LDD implant.



(a)



(b)

Figure 6.5 Comparison of the electric field in a MOSFET with or without the LDD

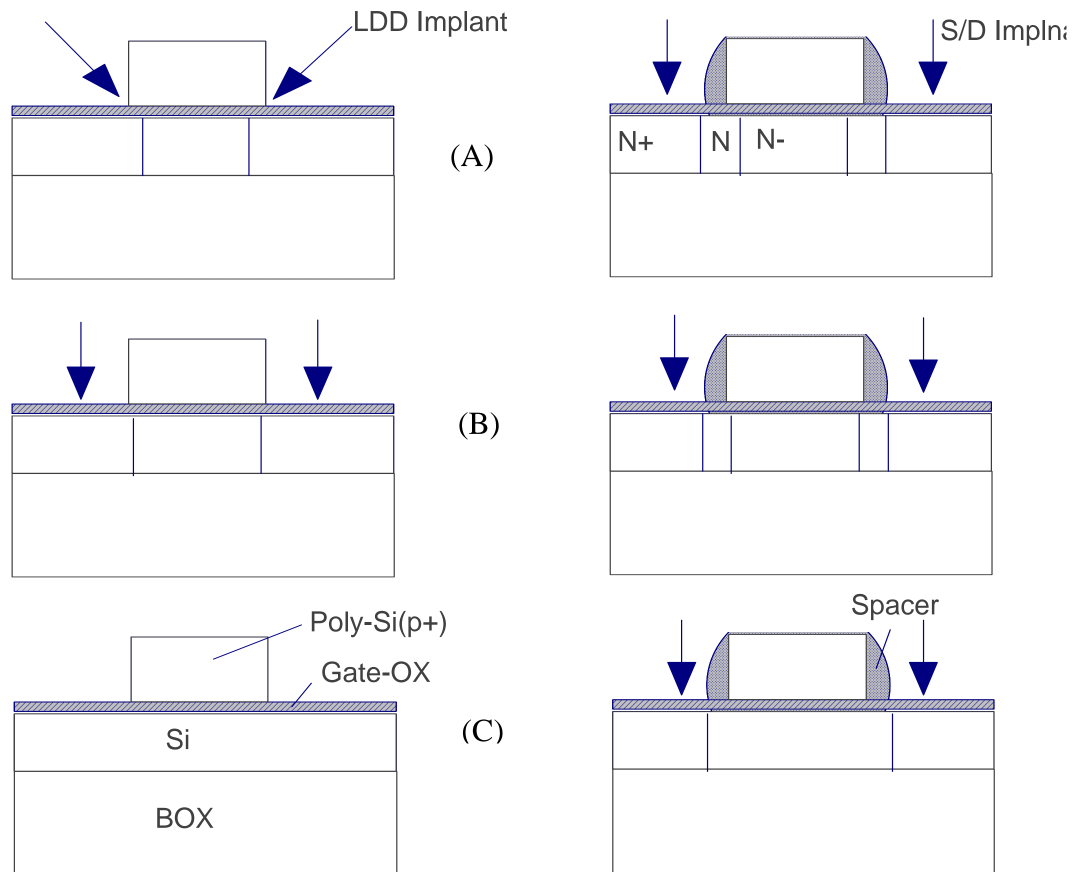


Figure 6.6 Simplified process flow for the three LDD designs (A), (B), and (C) described in the text. Structure (A) incorporates a large angle LDD implant, structure (B) a zero angle implant, whereas structure (C) does not use LDD implant.

Table 6.3: Summary of experimental results of the front and back channel transconductance degradation, hot carrier lifetime, latch-up voltage, and ring oscillator speed measurements of structures A, B, and C.

LDD Process / Parameter	A	B	C
$\Delta g_{m1}/g_{m1}$ (%)	0	2	9
$\Delta g_{m2}/g_{m2}$ (%)	4	4	7
Hot Carrrier Lifetime (s)	$3x10^8$	$1x10^8$	$7x10^5$
V_{DLU} (V)	3.40	3.55	3.80
Ring Oscillator Speed (Mhz)	17.7	16.9	16.7

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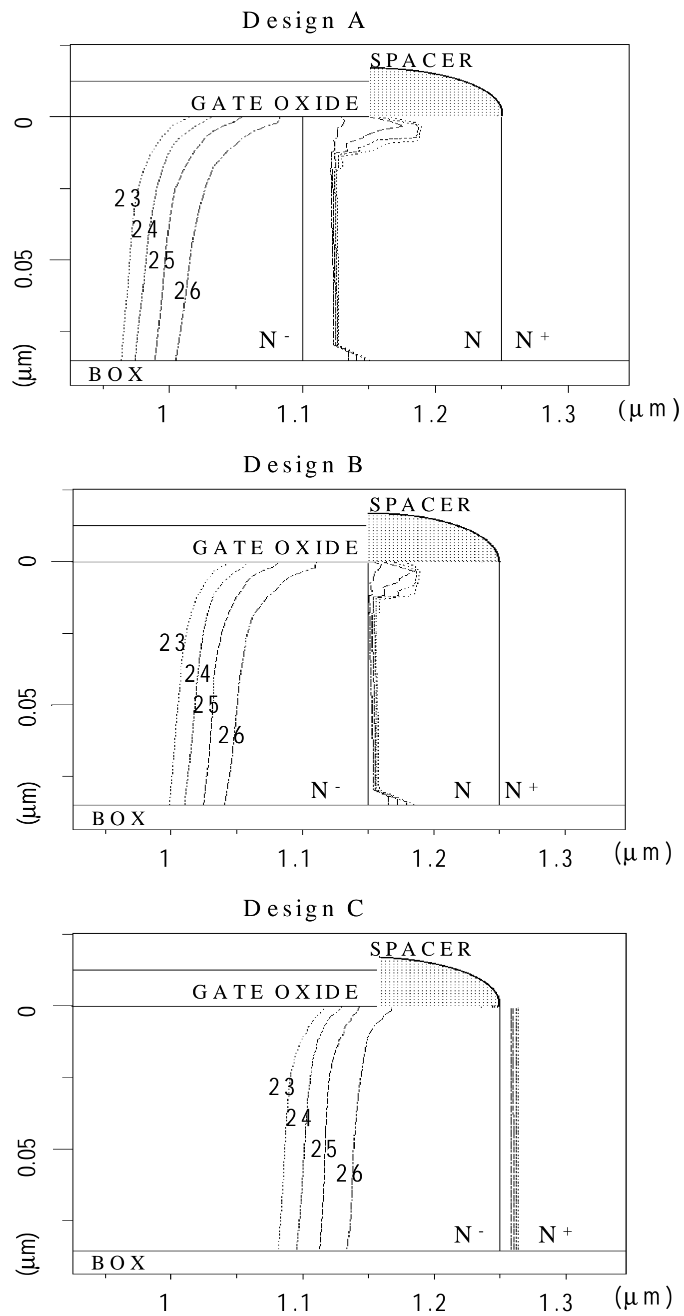

Figure 6.7 Contours of the impact ionization rate G (in logarithm ($cm^{-3}s^{-1}$)) during hot carrier stressing (V_{G1}=1.6V and V_D=3.2V) for structures A, B, and C. The location of the carrier generation with respect to LDD and spacer is in agreement with the observed device degradations.

Table 6.4 Integrated impact ionization generation rate along the top, middle, and bottom of the silicon film for structures A, B, and C under the bias V_{G1}=1.6V and V_D=3.2V. The averages of these three values are also given as a comparison to the measured latch-up voltages.

Structure	Impact Rate Integral ($1/cm^2$ s)				Latch-up Voltage (V)
	Top	Middle	Bottom	Average	
A	$8.5x10^{20}$	$1.7x10^{22}$	$2.9x10^{22}$	$1.6x10^{22}$	3.40
B	$8.0x10^{20}$	$8.2x10^{21}$	$2.3x10^{22}$	$1.1x10^{22}$	3.55
C	$7.9x10^{20}$	$1.5x10^{21}$	$1.8x10^{21}$	$1.4x10^{21}$	3.80

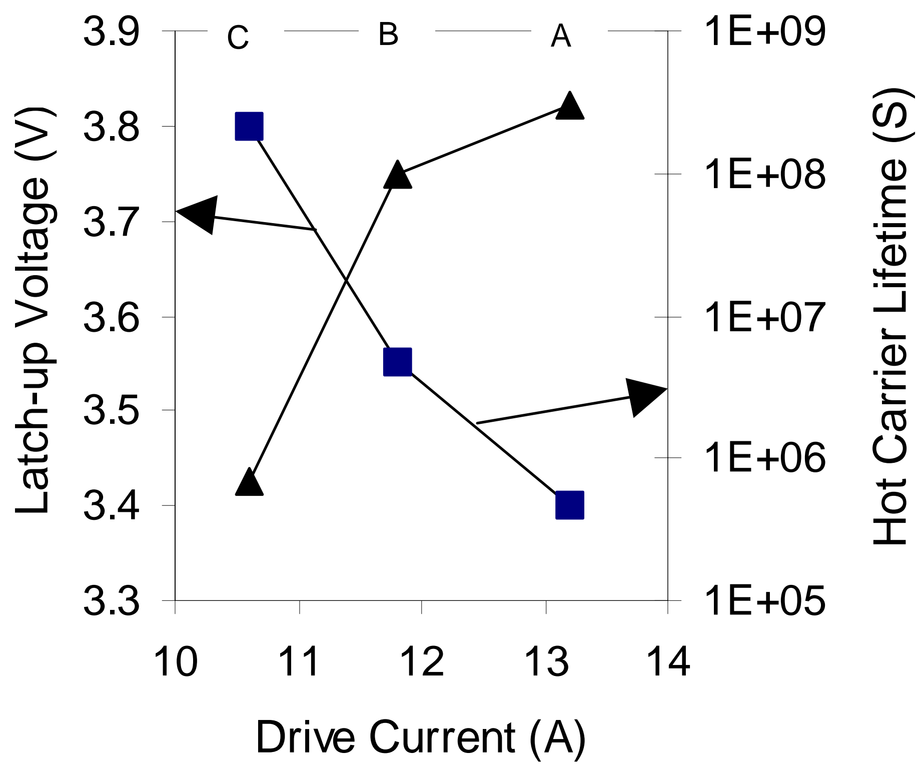

Figure 6.8 Tradeoff between drive current (measured at $V_G=V_D=3.3V$), latch-up voltage, and hot carrier lifetime. Best overall performance is obtained with structure "B".