

## ABSTRACT

### STUDIES ON CHANNEL COUPLING & FLOATING BODY EFFECTS AND THEIR EFFECTS ON DEVICE PERFORMANCE & RELIABILITY IN SOI MOSFET

Franklin L. Duan

George Mason University, 1998

Dissertation Director: Dr. Dimitris E. Ioannou

SOI MOSFET's is one of the promising options for the future VLSI market due to its low power/higher speed character and simplified technology with increased packing density. Yet some problems in device physics must be fully understood before SOI is implemented in industry. These problems are around the three basic features of SOI device: Two separate gates, channel coupling, and floating body effect. In this thesis, first an extensive study of the opposite-channel-based injection (OCBI) phenomenon is carried out by PISCIS numeric simulations. The results demonstrate that when stressing one channel, carriers can and are injected into the opposite gate. Under appropriate bias conditions pure hole/electron injection does take place. Secondly the hot carrier generation as a function of the different channel coupling was extensively studied by the aid of PISCES numeric simulation. Results show a trade-off between hot carrier degradation and the single transistor latch-up, i.e., stronger coupling ameliorates the carrier degradation but deteriorates the latch-up voltage. Thirdly a suitable two-dimensional structure was

conceived to simulate the three dimensional feature of the floating body effect. The simulations reveal that there is considerably higher carrier generation near the edges of the channel, and more so for wider devices. Fourthly, based upon the analysis of the existing two modes of FD SOI MOSFET, inversion mode and accumulation mode, a new mixed mode structure of FD SOI MOSFET is proposed, which holds the drawbacks of low channel mobility in the inversion mode and poor latch-up voltage in the accumulation mode. Moreover, the new device is more resistant to hot carrier degradation. Finally the compatibility of bulk technology in SOI was studied. Results show that the optimized LDD technology for bulk is not optimized in SOI due to its tradeoff between device reliability and the latch-up voltage.