

OBJECTIVE: Semiconductor Device Technology & Physics. Semiconductor Technology & Reliability, Technology Integration.

SUMMARY :

Semiconductor Technology Integration: 6+years experience on 'Memory Technology and Process Integration' from 0.18um to 90nm

Semiconductor Reliability: 2+ years experience on transistor / circuit reliability (HCI) from 90nm to 32nm

Misc. skills:

Computer: IC layout (TS) design, device and process simulation (SUPREM, PISCES), MS Office, Frame-maker, website design

Experimental: Semiconductor device measurement skill, Agilent 4156.

EDUCATION:

Ph.D., Electrical & Computer Engineering, George Mason University, VA. 1998, GPA 4.0.

Thesis: SOI device degradation and reliability study.

M.S., Electrical Engineering, Tsinghua University, Beijing, China. 1987, GPA 3.2

Thesis: Research on VLSI processes

B.Sc., Electrical Engineering, Tsinghua University, Beijing, China. 1985, GPA 3.3.

PROFESSIONAL EXPERIENCE:

AMD, Sunnyvale, CA

2005-2007

MTS, Technology Development Group, from 90nm to 32nm technology generation.

- Device and circuit HCI-related reliability, esp. on SOI. Technology generation from 90nm to 32nm. Reliability methodology development and technology qualification (90nm and 65nm)

LSI LOGIC, Milpitas, CA

1998-2005

Staff Engineer, Memory Technology and Process Integration, from .35um-90nm technology generation.

- SRAM layout and SRAM-related test structure design to ensure functionality, yield, and manufacturability. Develop and monitor inline process for SRAM integration on ASIC.

Ph. D RESEARCH, George Mason University, VA

1994-1998

Ph.D. Candidate, SOI device physics and reliability.

- Semiconductor device reliability studies and hot carrier degradations, esp. SOI devices. More details in publications below.

SINGAPORE TECHNOLOGY

1992

Process Engineer, Chartered Semiconductor Manufacturing

- Process integration and semiconductor chip manufacturing of 0.8um VLSI technology

INSTITUTE OF SEMICONDUCTORS

1987- 1992

Research Associate, Chinese Academy of Sciences, China

- Physics of superconductor devices and III-V compound semiconductors.

PROFESSIONAL SKILLS:

Semiconductor Testing:

- Designing proper test structures for transistor / circuit characterization, for SRAM design rule validation, and for reliability assessment.
- Device / circuit characterization and reliability test on wafer- and package-level using single-site and multi-site test system.

Semiconductor Process:

Process integration, esp. memory technology integration in ASIC, starting from 0.35um to 90nm generation.

Computer /Equipment Skills:

- Semiconductor device measurement skill using HP 4156. Computer Aided Measurement on HCI, data collecting and control. Interface language programming on electronic equipment like HP4145 and HP Pulse Generator by PC.
- IC Layout design tools. Semiconductor simulation tools, including process simulation--SUPREM, device simulation--PISCES.
- Web page design tools, search engine optimization tools.

AWARDS AND HONORS: 1995, 1997 Fellowship in George Mason University

PROFESSIONAL MEMBERSHIP: IEEE Membership since 1992 – 2005

REFERENCES: Available upon request

Patents:

1. Reduced soft error rate (SER) construction for integrated circuit structures, issued 2002
2. Single channel four transistor SRAM, issued, 2002
3. A new method to detect random and systematic transistor degradation for transistor reliability evaluation in high-density memory – 2003
4. Method and apparatus for characterizing shared contacts in high-density SRAM cell design – 2003
5. New methodology to measure many more transistors on the same test area – 2007

Publications**Most Recent:**

1. "Impact of Monitoring Voltage on the Lifetime Extrapolation During the Accelerated Degradation Tests", IIRW2006. Franklin Duan, Stephen Cooper, Amit Marathe, John Zhang, Sankaran Kartik Jayanarayanan.
2. "Design and Use of Memory-Specific Test Structures to Ensure SRAM Yield and Manufacturability", ISQED'2003, pp119-124, F. Duan, R. Castagnetti, R. Venkatraman, O. Kobozeva, and S. Ramesh, LSI Logic Corporation, 2003
3. "High-Density and High-Performance 6T-SRAM for System-on-Chip in 130 nm CMOS Technology", W. Kong, R. Venkatraman, R. Castagnetti, F. Duan and S. Ramesh, VLSI Symposium, 2001.

Previous:

1. Franklin L. Duan, Dimitris E. Ioannou, Shankar P. Sinha, and Frederick T. Brady, "LDD Design Tradeoffs for Self Latch-Up and Hot Carrier Degradation Control in Accumulation Mode FD SOI MOSFET's", *IEEE Transactions on Electron Devices*, vol. 44, pp.972-977, 1997.

2. F.L. Duan, X.Zhao, D.E. Ioannou, H.L. Hughes and S.T. Liu, "Detrimental Edge Effects on the Floating Body Phenomena in SOI MOSFETs", *Symposium of 192nd International Meeting of the Electrochemical Society, Inc.*, pp.239-245, 1997.
3. Franklin L. Duan and Dimitris E. Ioannou, "Design and Analysis of a Novel Mixed Accumulation/Inversion Mode FD SOI MOSFET", *1997 IEEE International SOI Conference Proceedings*, pp.100-101, 1997.
4. Franklin L. Duan, Dimitris E. Ioannou, Harold L. Hughes and Mike Liu, "Channel Coupling Imposed Tradeoffs Between Hot Carrier Degradation and Single Transistor Latch-Up in FD SOI MOSFET's", *IEEE International Reliability Physics Symposium*, pp.194-202, 1998.
5. Dimitris E. Ioannou, Franklin L. Duan, Shankar P. Sinha, and Andrej Zaleski, "Opposite-Channel-Based Injection (OCBI) of Hot-Carriers in SOI MOSFET's: Physics and Applications", *IEEE Transaction on Electron Devices*, vol.45, May 1998.
6. D.E. Ioannou, F.L. Duan, and X. Zhao, "SIMOX Substrate and MOSFET's for Enhanced Reliability and Performance", *1997 International Semiconductor Device Research Symposium*, pp.627-630, 1997.
7. Dimitris E. Ioannou, Franklin L. Duan, Williams C. Jenkins, and Harold L. Hughes, "Channel Coupling Imposed Tradeoffs on Fully-Depleted (FD) SOI MOSFET's", *submitted to ESSDREC'98*.
8. X. Zhao F.L. Duan, A. Thanailakis, D.E. Ioannou, R.K. Lawrence, and H.L. Hughes, "Hole Trap Investigation in Supplemental Oxygen SIMOX Wafers by Opposite Channel Based Charge Injection", *1997 IEEE International SOI Conference Proceedings*, pp.116-117, 1997.
9. Shankar P. Sinha, Franklin L. Duan, Dimitris E. Ioannou, William C. Jenkins, and Harold L. Hughes, "Time Dependence Power Laws of Hot Carrier Degradation in SOI MOSFET's", *1996 IEEE International SOI Conference Proceedings*, pp.18-19, 1996.
10. S. P. Sinha, F.L. Duan, D.E. Ioannou, William C. Jenkins, Harold L. Hughes, and M.S. Liu, "Hot Carrier Degradation of Fully Depleted SIMOX MOSFET's", *Proceedings of the 7th International Symposium On Silicon-On-Insulator Technology and Devices*, pp.324-329, 1996.